INSTITUTE OF ELECTRONICS AND COMPUTER SCIENCE

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New precise timing solutions and their application in JUNO project

Jauni precīzā laika risinājumi un to izmantošana JUNO projektā

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“High precision synchronous timing in widely distributed scientific instrumentation”

Presentation Scope

Local Clock Distribution System (LCDS)

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CCDU realization and obtained specifications

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Local Clock Distribution System (LCDS)

LCDS is intended for industrial or scientific experimentation systems that are used to collect timing information from multiple sensors, which are remote and specially distributed. Such systems very often have time measurement devices (event timers or, in other words, time-tagging devices), which sit close to each sensor. Each time-tagging device has its own local time-scale.

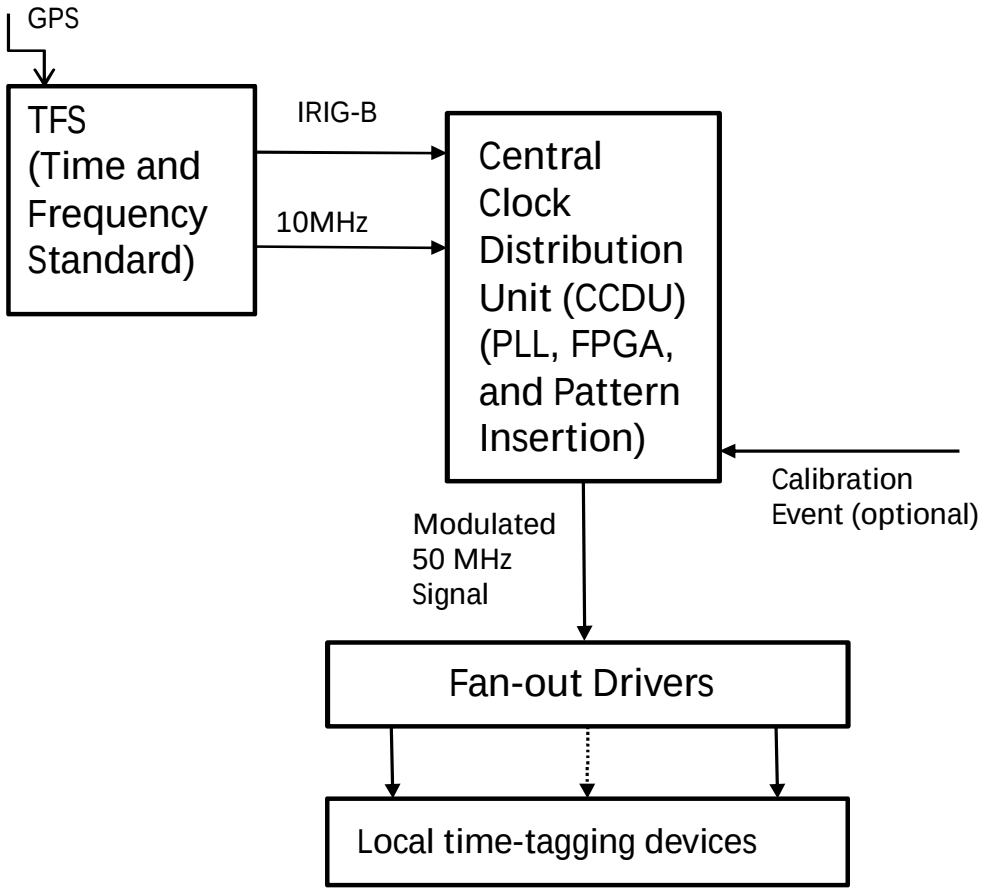
The signals from the sensors that are regarded as informative events are time-tagged and then the obtained time-tags are transmitted to some central data acquisition unit. The time-tags that are related to different sensors later have to be placed on some single system time scale so as to be correctly processed for the experimental or industrial needs. Sometimes it is needed to have the time-tags associated with the UTC (Universal Time Coordinated).

The proposed LCDS has to cover the above mentioned needs and provide the following functionality:

1. Provision of the stable synchronous clock for all local time-tagging devices.
2. Synchronization (syntonization) of all local timescales of the local time-tagging devices.
3. The calibration of the timing offsets between all measurements channels (global calibration).

And additionally:
4. Provision of a System Time Scale, which is synchronized with the UTC.
5. Absolute timing calibration. It means that all timestamps from different channels have to be UTC associated.

The LCDS consists of the following main blocks: Time and Frequency Standard (TFS, often it is called Time and Frequency Reference), Central Clock Distribution Unit, Fan-out drivers, and Local Time-tagging Devices (strictly speaking they are not part of the system, shown only for the clarity of the description).

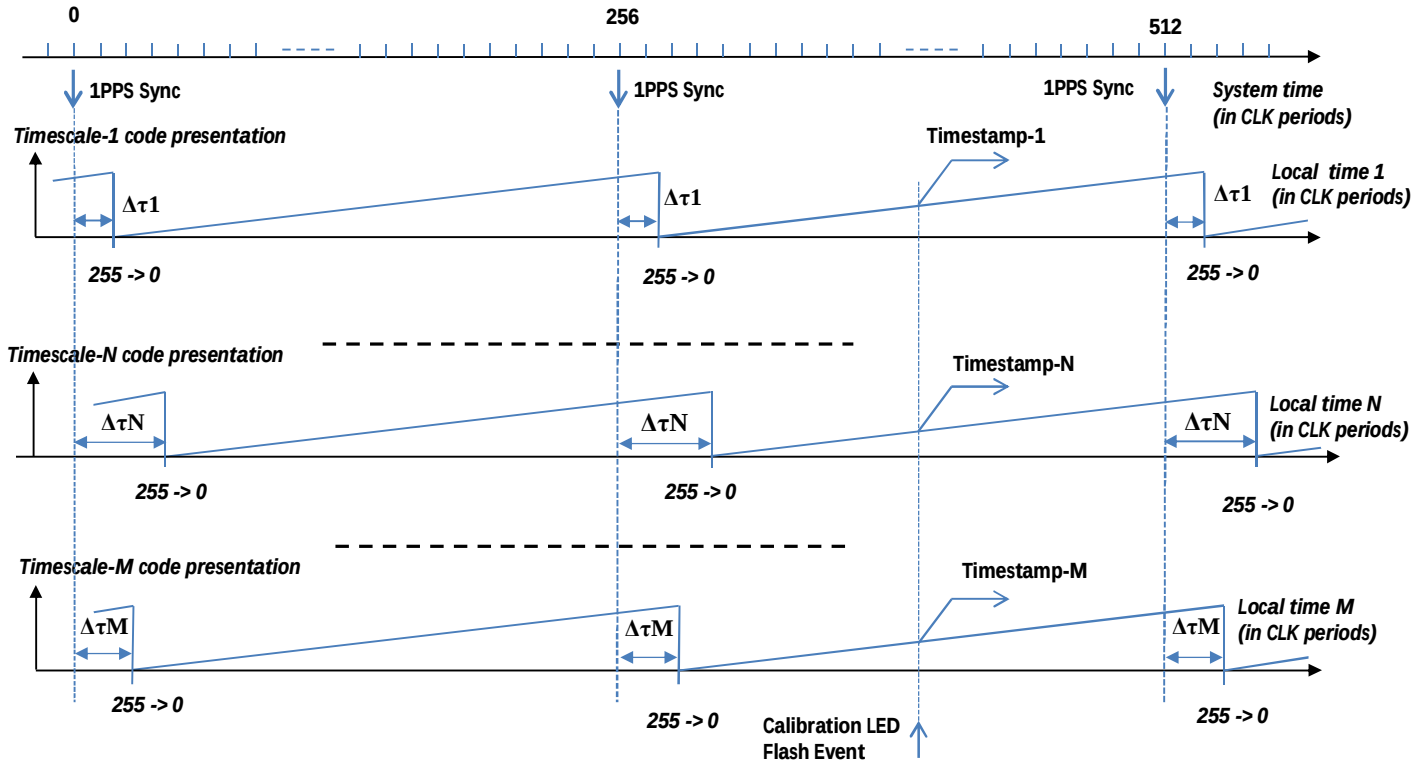


The operation of the system is based on the use of a TFS. The TFS produces a stable clock signal (10 MHz as a rule) alongside with the Time Code signal (IRIG-B standard is suggested to be used as one of most popular). Such device normally can be disciplined from the GPS network and is usually based on a Rubidium standard or a TCXO (temperature compensated crystal oscillator).

The CCDU produces a very stable and low jitter 50 MHz clock signal that is farther distributed by Fan-out Drivers. Upon the reception of the time code from the TFS the CCDU inserts a specific code pattern in the 50 MHz. The local time-tagging devices use the 50 MHz signal to build their internal time-scales.

The synchronization (strictly speaking – syntonization) is done with the use of the inserted time codes that are repeated (typically – once in a second). The time code contains the current UTC time, a specific edge of the pattern indicates the 1PPS signal. The local time-taggers have to be equipped with Clock and Data Recovery blocks that are PLL based and are able to extract time codes from the incoming 50 MHz signal.

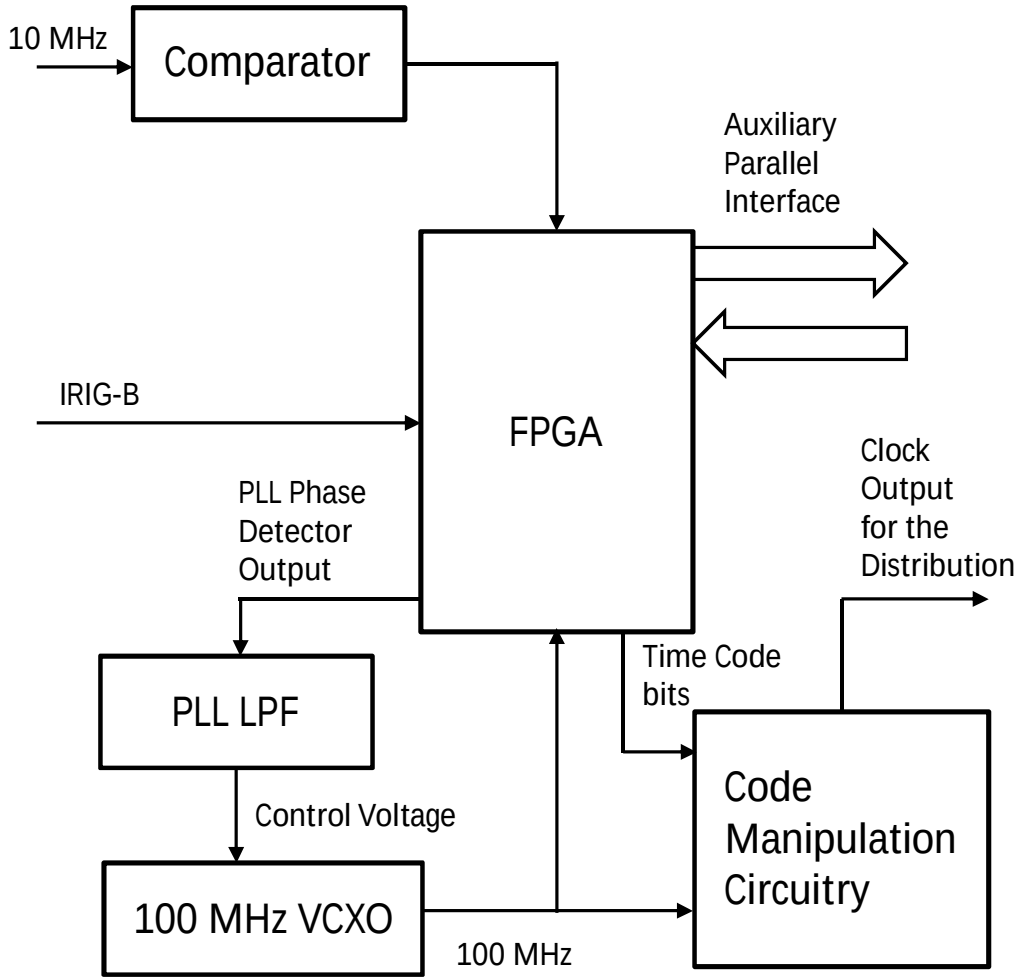
Because of different delays between the CCDU and the local time-tagging devices, the local time scales always have different time offsets between each other. Therefore to perform time-tagging of the events that are related to different local time-scales the global system calibration has to be performed. Normal way to do that is to generate a special physical pulse signal that has the impact on all sensors of the time measurement system. In optical systems, for example, such signal could be a flash of a laser or LED (Light Emitting Diode) that comes to all sensors. The spatial position of the calibration signal source has to be determined (or accurately measured).



The calibration events (caused by flashing the central LED) are time stamped by all local time-tagging devices with respect to their local timescales. These timestamps (Timestamp-1,..., Timestamp-n,..., Timestamp-M) are offset with respect to one another. And not only the offsets between the local timescales get included in those offsets of the timestamps, but also the different delays along the optical-electronic paths of LED Flash Event before the timestamps are taken by different local time-taggers (optical length delays, delays of the front-end sensors, delays of input amplifiers, etc.). So, all delays are included and can be taken into account by means of the Global Calibration. This way all time-tags from local time-taggers become related to some single system local time-scale, which, it its turn, can be associated with the UTC.

Central Clock Distribution Unit Description

A compact implementation of the CCDU is based on the use of a generic FPFA. The CCDU consists of: a Comparator, an FPGA, a PLL Low Pass Filter (PLL LPF), a 100 MHz VCXO, and Code Manipulation Circuitry (CDC).



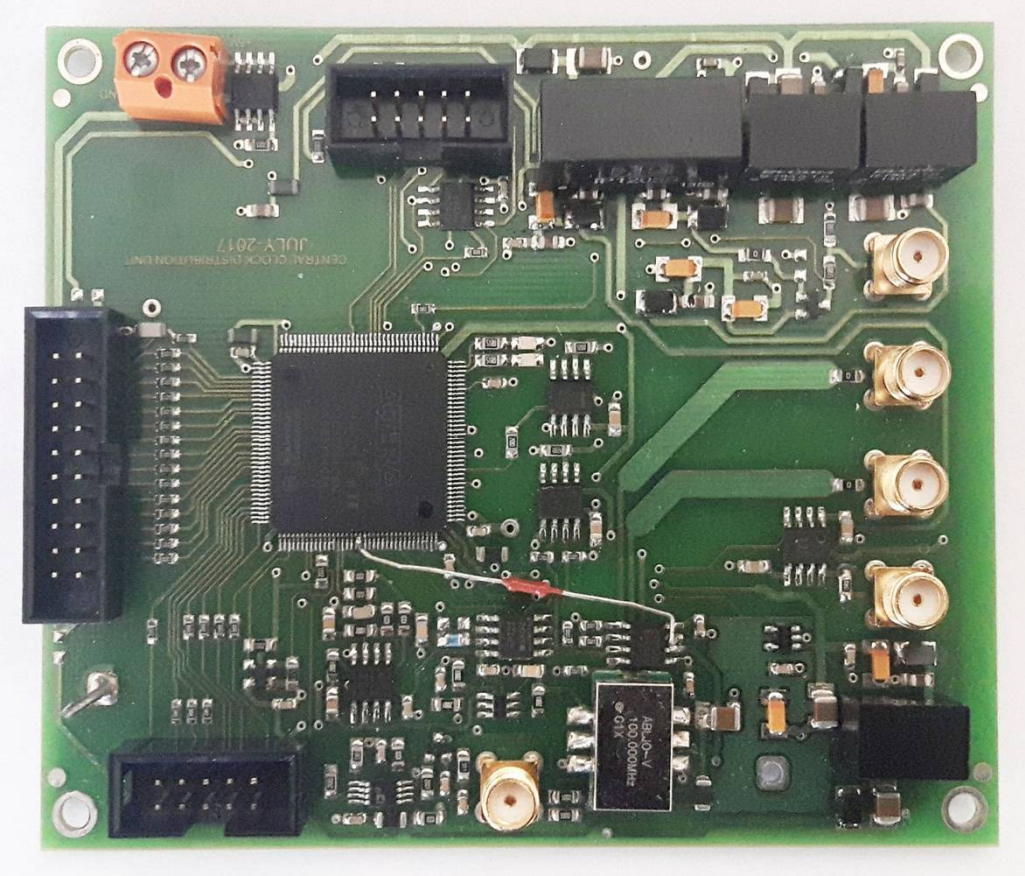
The Comparator performs the signal conditioning of the 10 MHz input signal (it could be a pulse or sinusoidal signal with different amplitude). The LVTTL signal from the output of the Comparator comes to the FPGA.

The generation of the 100 MHz on-board internal clock (up-conversion of the 10 MHz to 100 MHz) is done by the PLL circuitry, which is implemented inside the FPFA. Only PLL LPF is done outside the FPFA. The PLL LPF produces the control voltage for the 100 MHz VCXO to obtain the locked loop. As a result the obtained 100 MHz clock signal is synchronized to both the input 10 MHz signal and the IRIG-B signal.

The 100 MHz clock is fed both to the FPGA and the Clock Manipulation Circuitry. The CMC implemented on a D-type flip-flop circuitry. When IRIG-B 1PPS signal comes, it is processed by the FPGA that inserts a specific pattern into the output clock by the provision of information bits (which come to the D-input of the main flip-flop of the CDC).

CCDU realization and obtained specifications

The CCDU is implemented as a single board 90mm x 107mm . The Altera CycloneII FPGA (EP2C5T144C7) is used. The board can be used in different distributed time-tagging systems and adjusted for the use of different distributed clock frequencies. The distributed clock frequency depends on the selected VCXO frequency and clock division coefficients that could be modified in the VHDL code for the FPGA.



The main specifications of the designed board are:

- Reference signal (10 MHz) input – AC, 50 Ohm input impedance, 100mV-10V peak-to-peak
- IRIG-B input – LVTTL, 50 Ohm input impedance
- Auxiliary parallel interface – LVTTL
- Auxiliary system clock output – differential LVPECL
- Output distributed clock signal – LVTTL, 50 Ohm diving capability
- Output clock signal jitter – less than 3 ps
- Distributed clock frequency range – 10-200 MHz
- Time code insertion format – IRIG-B
- Size - 90mm x 107mm
- Power supply +5V, 450 mA

The board was tested and showed reliable operation. The distributed clock jitter was measured indirectly by the use of two test 100 MHz PECL outputs (differential signals). These signals were connected to the main board of the Eventech A033-ET (high accuracy event timer with the time-tagging RMS resolution less than 2 ps) and used as the system clock of that event timer. Then time measurements (by the A033-ET) of a low jitter pulse signal were carried out.

The results showed a small time-tagging RMS resolution degradation (3 ps instead of the specified 2 ps), which means that the jitter of the CCDU system clock is less than 3 ps (based on the assumption that the A033-ET is "ideal" and introduces no measurement error, which is not true). So, in the reality, the jitter of the CCDU clock is noticeable lower. But this guaranteed figure of jitter is much better then typically required.

As a rule the distributed clock signal degrades in the transmission lines and driving/receiving circuitry and then the jitter is improved in the CDRs of local time-taggers (the degree of such improvement depends on the application).

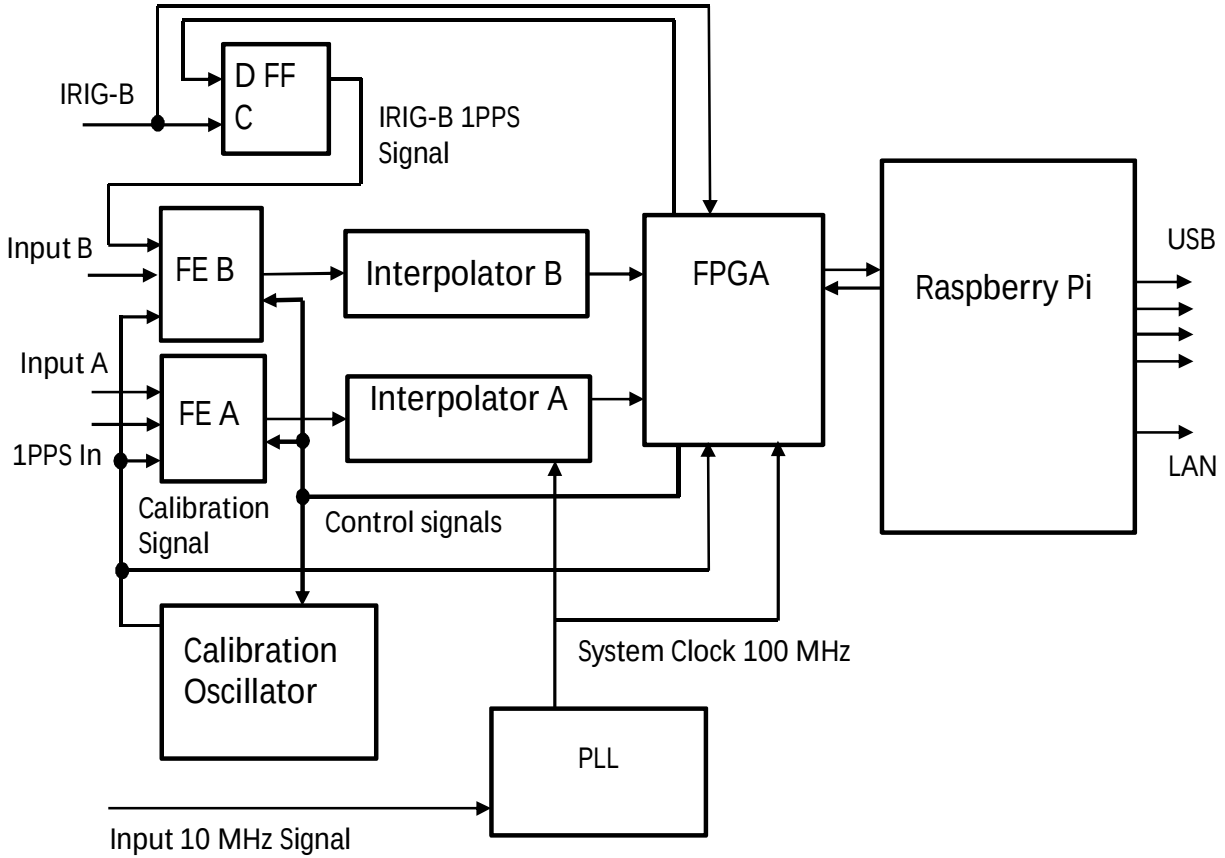
True Event Timer (TET)
(project)

The TET is a true event timer, which is able to perform time tagging of events (represented by electrical pulses) with very high accuracy with respect to its internal time scale. The Module's time scale can be synchronized with the UTC (using 1PPS/IRIG-B signal and 10MHz reference) so as the user could do the event time tagging with respect to that universal time scale. The TET could be connected to the White Rabbit network by means of WR-LEN (White Rabbit Lite Embedded Node from Seven Solutions) or a similar node.

The TET is intended for use in KHz SLR (Satellite Laser Ranging), Time Transfer, nuclear physics, 2D/3D scanners, laser altimetry, LIDARs, as well as for other applications that require accurate time measurements. In particular, the TET is intended for time tagging of various events with high accuracy during the JUNO experiment.

Principles of Operation of the TET

The TET consists of the following functional blocks: Front End (FE) A and B, Interpolator A and B, FPGA controller, PLL, Calibration Oscillator, Synchronization Flip-flop (FF) and RASPBERRY Pi.



In the normal measurement mode the TET accepts input events that come as electrical pulses at the inputs A and B. Positive edges of these pulses are regarded as events. The input pulses come to the Interpolator blocks (through the Front End blocks), where the time intervals between the pulse active edges and the following 100 MHz system clock signal edges are estimated. As a result the Interpolators send to the FPGA the raw data, which contain the information about those time intervals. In other word, these data carry the information about the fraction of the system clock signal period, which corresponds to the moments of the events.

The FPGA performs internal digital processing of the obtained data so as to produce the binary codes of those fraction time intervals. This way the high accuracy estimation of the time of events within the 100 MHz clock period is carried out (fine time-tagging).

The coarse time-tagging is done by means of a counter of system clock signal – coarse time scale counter. When the data about an event comes from the interpolators, the state of the coarse time scale counter is read; the complete time tag code is assembled from the coarse time tag code and the corresponding fine time tag code. The assembled time-tags are taken by the on-board computer (Raspberry Pi) as they appeared in an internal memory buffer. An application-specific part of the Rasspberry SW provides data transmission (via USB or LAN) or processing and presentation at visualization devices (LED panel, monitor etc.).

The coarse time scale can be synchronized with the UTC by means of the IRIG-B time code signal, which comes directly to the FPGA. Because of various electronic component delays and other factors there is always an offset between the UTC and the TET's local time scale. For estimating this offset the time-tagging of the 1PPS signal is used. Two possibilities to do so are covered by the TET.

The first possibility is supported by a direct 1PPS input (of the Front End A). In the 1PPS time-tagging mode the 1PPS input is enabled, the obtained time-tags of 1PPS signal are used for the TET's local time scale offset (with respect to the 1PPS signal) calculation. Obviously, the accuracy of the estimation of the TET's time scale offset with respect to the UTC is determined by the accuracy of an employed 1PPS signal.

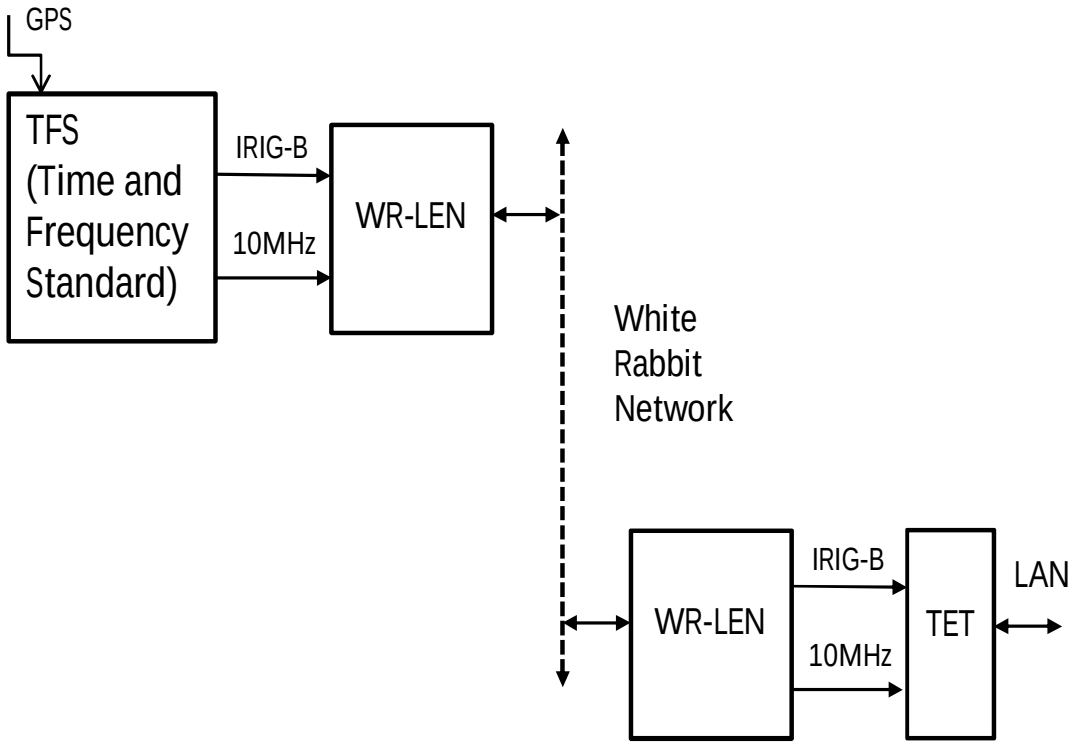
The other possibility to time-tag the 1PPS signal is to extract the edges, which correspond to 1PPS edges, from the IRIG-B signal. The D-type Flip-Flop block is used for that purpose. The FPGA analyses the incoming IRIG-B signal and produces Flip-Flop enable signals (at the D inputs) one IRIG-B clock period in advance to the 1PPS edge of that signal so as to obtain a pulse (IRIG-B 1PPS signal, see the block diagram) corresponding to that edge.

The Interpolator circuitry always has certain nonlinearity (or, in other words, the transfer function of the Interpolators is non-linear). To rectify that, a specific calibration procedure has to be carried away. The calibration is done by time-tagging the calibration signal that is generated by the Calibration Oscillator. In terms of statistics the transfer function of the interpolator can be obtained if the calibration signal events are uniformly distributed within the 10 ns system clock period.

For obtaining such distribution, a stable low jitter voltage-controlled crystal oscillator with a specifically chosen determined frequency (with respect to the system frequency) is utilized. The chosen frequency is maintained with high accuracy by means of FLL (Frequency Locked Loop) circuitry that is based on the 1.544 MHz VCXO and the FPGA VHDL control code. The FPGA continuously measures the frequency of the calibration VCXO and, depending on the error sigh, correspondingly changes the VCXO's frequency by changing its control voltage (Digital-to-Analog Converter is used for this purpose).

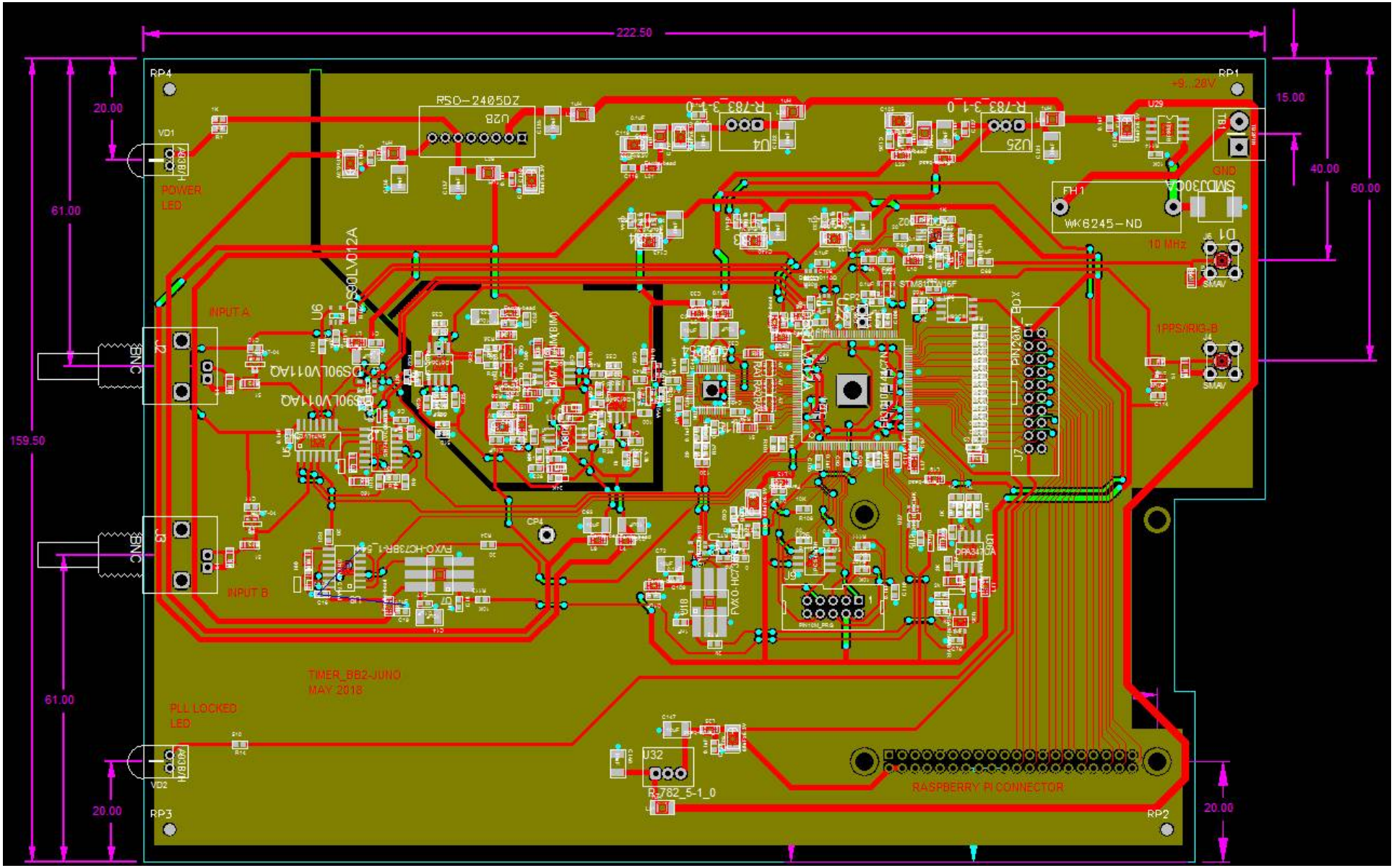
The system 100 MHz clock is derived from an input reference frequency signal 10 MHz by means of Phase Locked Loop circuitry that is based on a very low jitter VCXO.

Both the reference 10 MHz signal and IRIG-B/1PPS signal are normally provided by specific instruments – GPS-based Time and Frequency Standards (TFS). The TET can be either directly connected to a TFS or via the White Rabbit network. The WR-LEN (White Rabbit Lite Embedded Node from Seven Solutions) provides the necessary support for the distribution of the UTC.



The on-board computer of the TET should work in a network server mode and provide data packets that contain time-tag information.
The schematic of the TET has been captured and the PCB design has been done. It is planned to build a prototype in the spring this (2018) year.
It is planned to use WR-LEN modules Seven Solutions). As a TFS the GMR1000 (from MASTERCLOCK, Inc.) is planned to employ.

PCB design of the TET



Expected Features of the TET

- Two independent measurement channels A and B
- RMS resolution of time-tagging – 5-6 ps
- "Dead" time for each channel – 80 ns
- Dedicated input for the 1PPS signal
- Dedicated input for the IRIG-B signal
- Input to input offset drift (for all inputs) – expected about 15 ps/ºC
- Single input offset drift – expected about 15 ps/ºC
- On-board high quality (low jitter) PLL that derives the system clock (100 MHz) from an external 10 MHz reference source
- On-board computer RASPBERRY Pi
- Communication – Ethernet, USB-2
- Power supply - +9…28V, 3 W

The TET is housed in a small aluminium case 60x170x220 (from Hammond Manufacturing).

Conclusions

An original clock and time distribution system, which is based on an UTC specific code pattern (UTC time code) into the distributed clock, has been designed. The main block of the system has been built and tested. The high accuracy (less than 100 ps) and low jitter (less than 3 ps) of the distributed clock and time have been obtained.

A multifunctional True Event Timer (TET) has been designed. The TET could be used as a stand alone device, be used with the proposed clock distribution system, and with White Rabbit time and clock distribution systems.

The TET is designed as a low cost device and is characterized by high accuracy performance (time-tagging RMS resolution – 5…6 ps). Specific fast calibration procedure, which is built into the device's FPGA VHDL code has been designed. That allows supporting high performance of the TET in the wide temperature range.