ASYNCHRONOUS FIR FILTERS: TOWARD A NEW DIGITAL SIGNAL PROCESSING CHAIN

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Outline

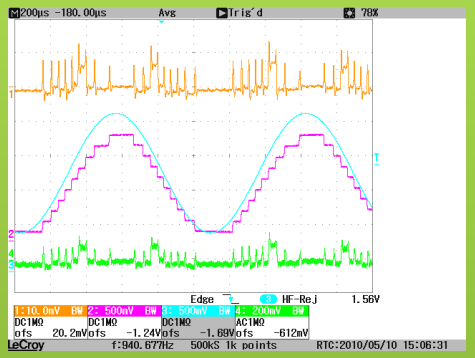
- Asynchronous logic
- Non uniform sampling
- Asynchronous convolution product
- Asynchronous FIR filter
- Conclusion and prospects

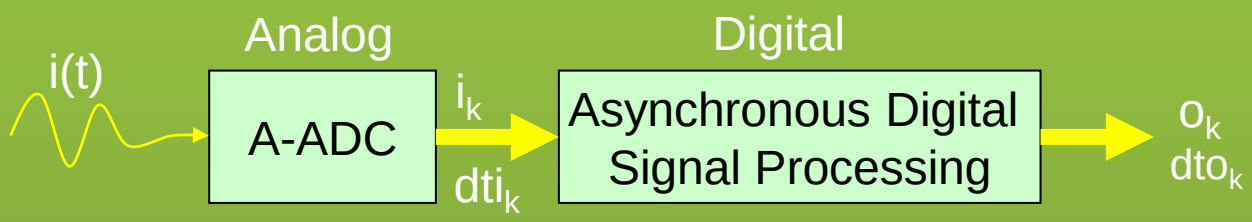
Asynchronous Logic

Why asynchronous logic ?!

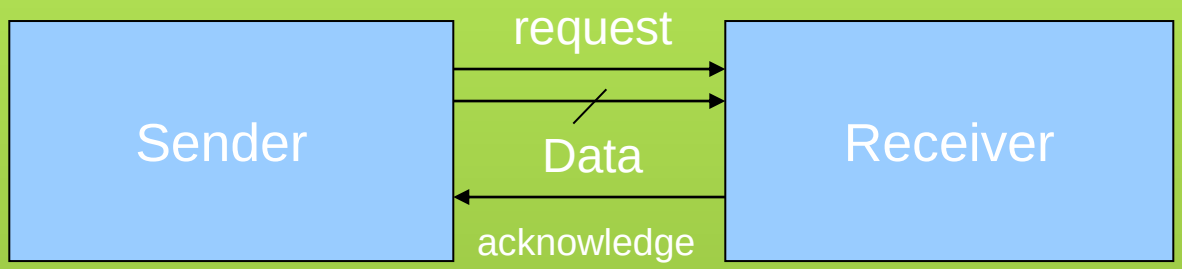
- Asynchronous systems are only driven by the signal information
- No global clock
- No activity when no data to compute

→ Low power consumption





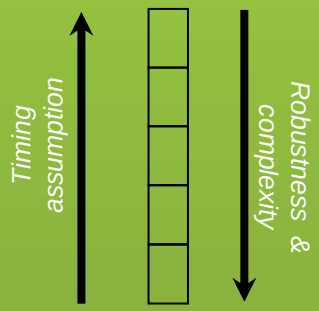
Asynchronous Logic – Basics



Handshake communication protocol

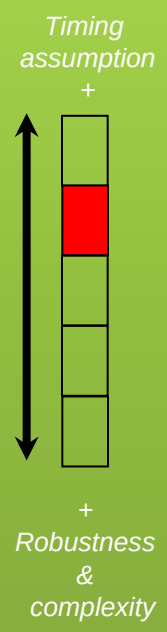
5 styles of asynchronous circuits:

- Delay insensitive circuits (DI).
- Quasi Delay insensitive circuits (QDI).
- Speed independent circuit (SI).
- ***Micropipeline.***
- Huffman.

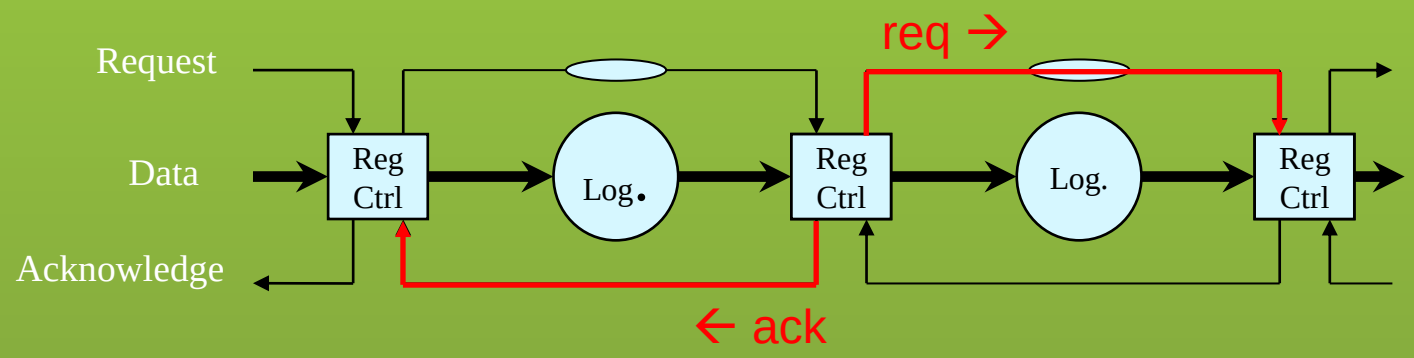


Asynchronous Logic – Micropipline

Asynchronous – Micropipeline circuits :



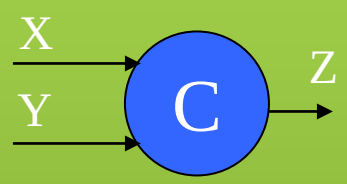
- Communication between different stages is based on Handshake model.
- Locally: worst case approach.
- Need a local timing assumption.



Asynchronous Logic – Muller gate

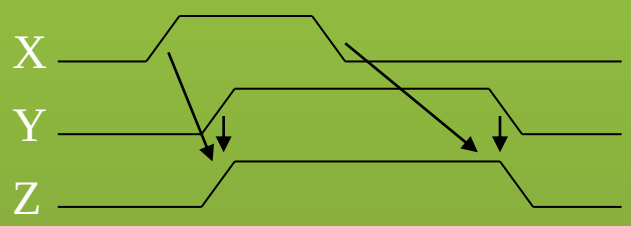
C-Element or Muller gate:

Symbol



Truth table

X	Y	Z
0	0	0
0	1	Z^{-1}
1	0	Z^{-1}
1	1	1



$$Z = XY + Z(X+Y)$$

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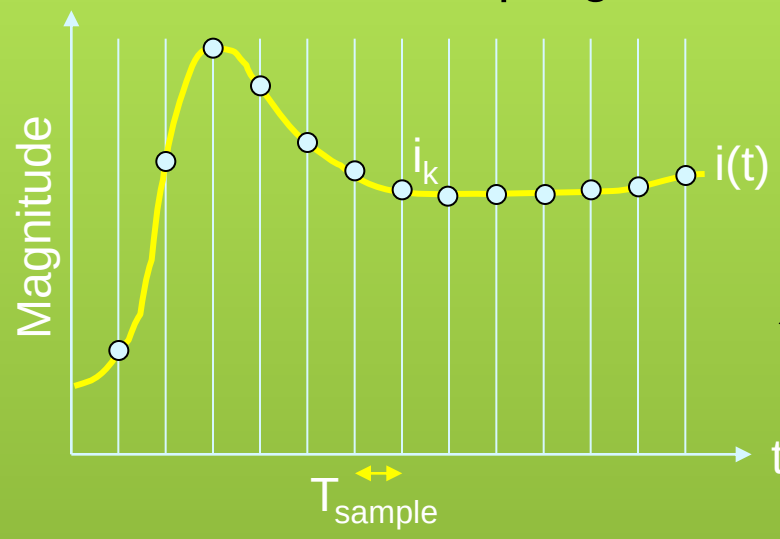
Non-uniforme Sampling

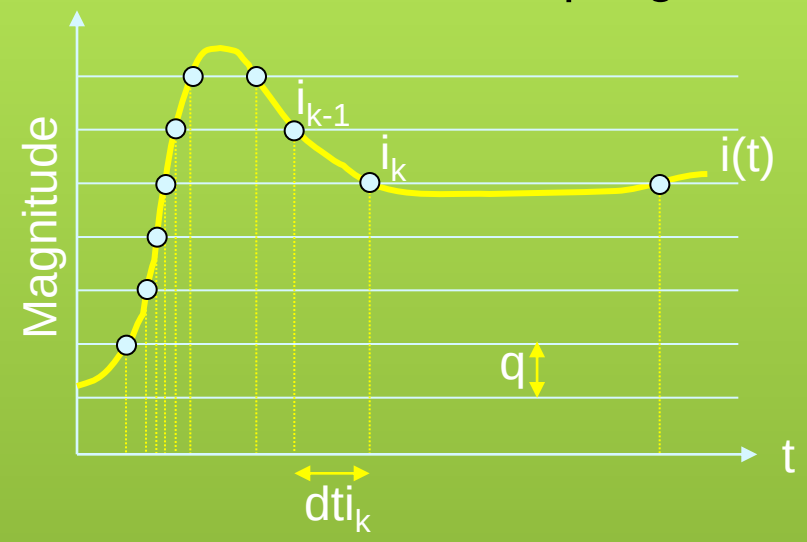
Non-uniform sampling

Uniform sampling



Dual

Non uniform sampling

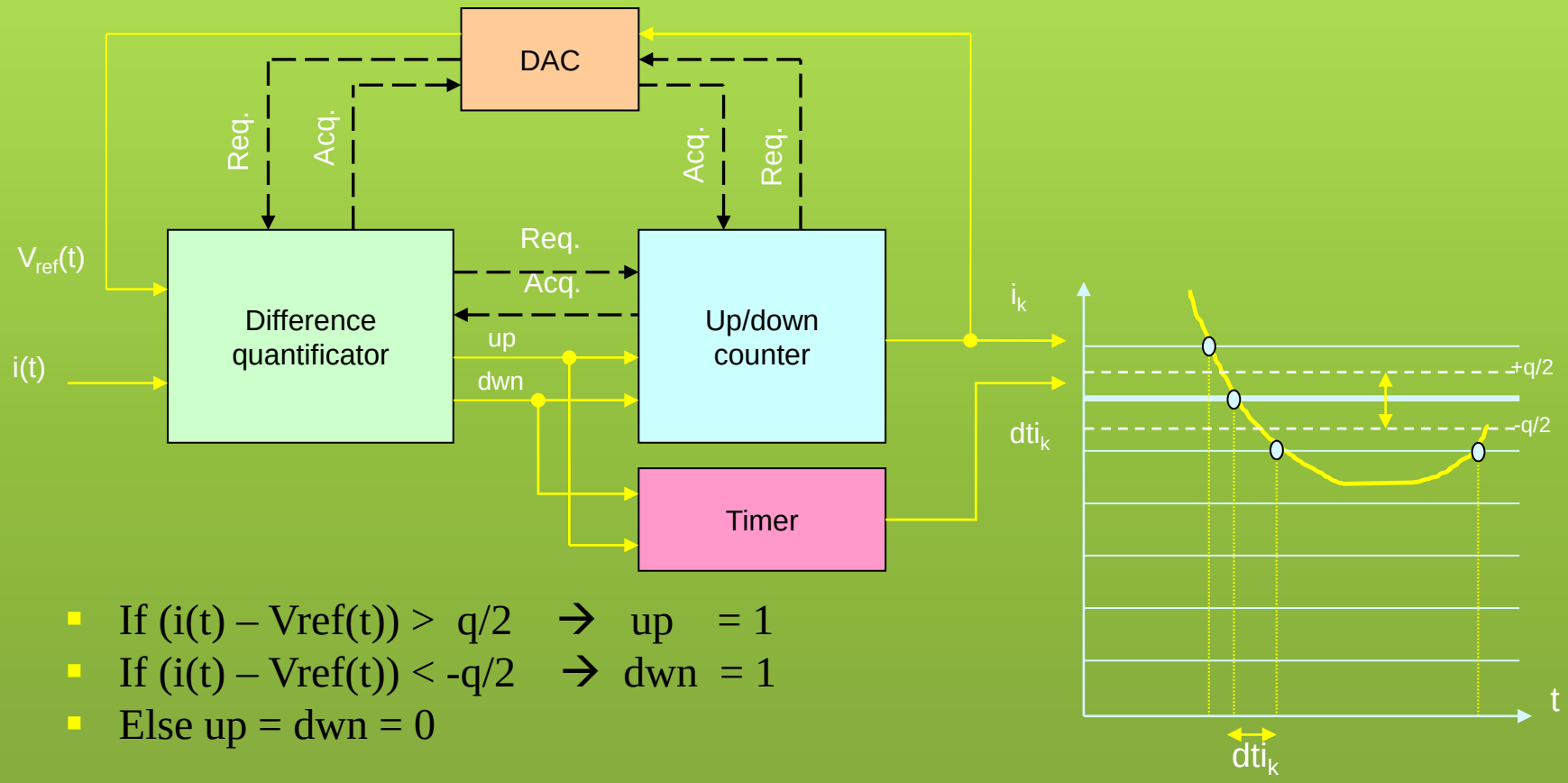


- *Respect the Shannon theorem*
- *Instants exactly known*
- *Information: T_{sample}, { i_k }*
- *In an ADC: Amplitude quantization*
- *Many useless samples*

- *"Level-crossing sampling"*
- *Amplitudes exactly known*
- *Information: quantum, { dti_k }*
- *In an A-ADC: Time quantization*
- *Only useful samples*

Non-uniform sampling – A-ADC Converter

A-ADC: Asynchronous design for Non uniform sampling



- If (i(t) – Vref(t)) > q/2 → up = 1
- If (i(t) – Vref(t)) < -q/2 → dwn = 1
- Else up = dwn = 0

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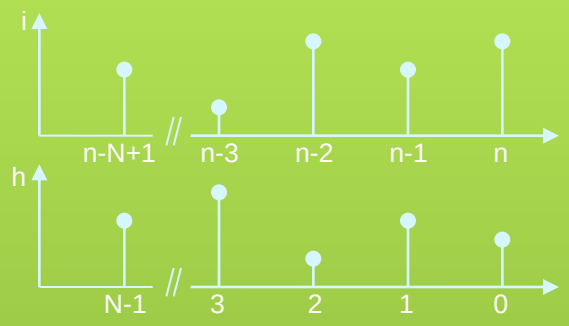
Async. convolution product

Convolution product – synchronous approach

$$o(n) = \sum_{k=0}^{N-1} h(k)i(n-k)$$



The instants are synchronized

Classical digital convolution product
incompatible with non uniformly sampled signals

Find a digital equation using the information
contained in the time intervals

Convolution product – asynchronous approach

- Asynchronous convolution product:

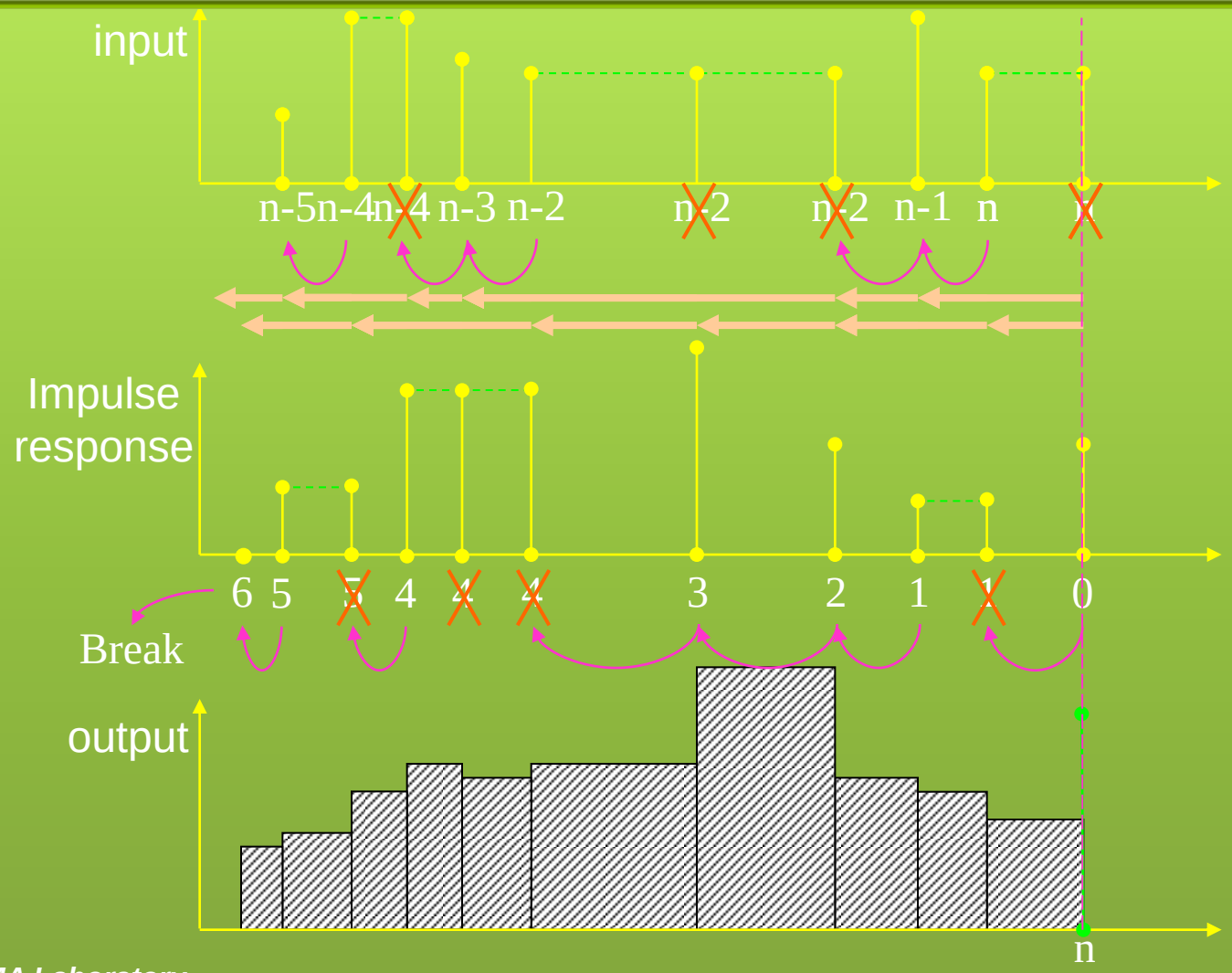
$$o(t) = \int_{-\infty}^{+\infty} h(\tau) i(t-\tau) d\tau \quad \Rightarrow \quad o(t_n) = \int_{-\infty}^{+\infty} \hat{h}_n(\tau) \hat{i}_n(t_n - \tau) d\tau$$

- Asynchronous convolution algorithm:

$$\begin{cases} o_n = \sum \min(dti_{n-k}, dth_j) i_{n-k} h_j \\ dto_n = dti_n, \end{cases},$$

- if $\min = dti_{n-k}$ then $dth_j = dth_j - dti_{n-k}$;
  $k = k + 1$,
- if $\min = dth_j$ the n $dti_{n-k} = dti_{n-k} - dth_j$;
  $j = j + 1$,
- if $\min = dth_j = dti_{n-k}$ then $k = k + 1$; $j = j + 1$.

Convolution product – asynchronous approach



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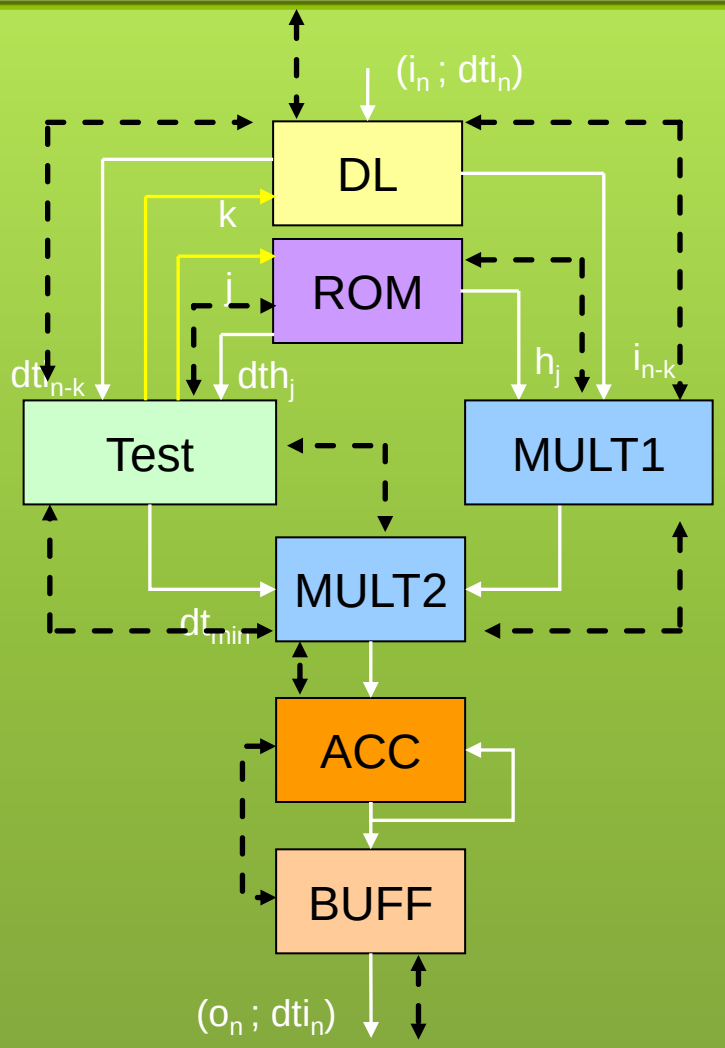
Async. F.I.R. product

Asynchronous F.I.R filter – The architecture

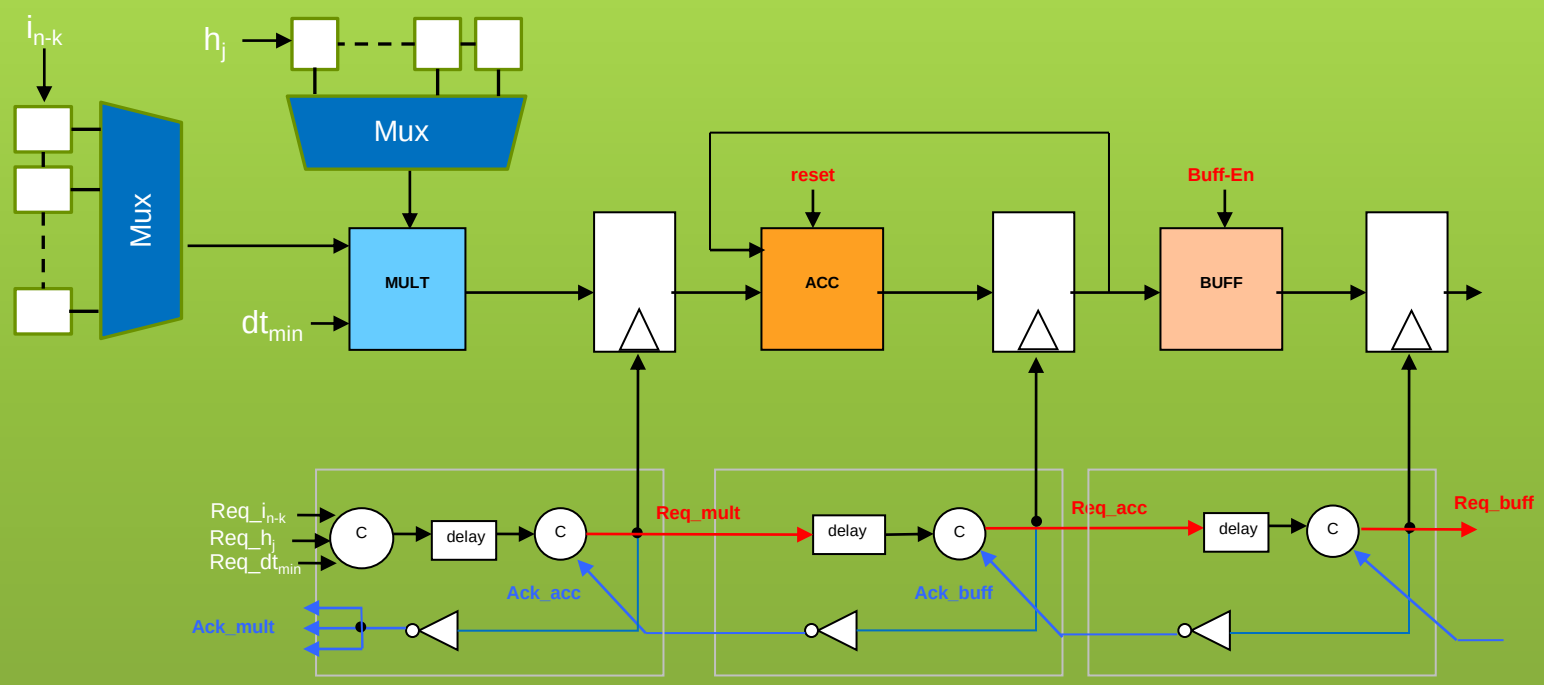
Architecture derived from the asynchronous convolution:

System triggered on signal events



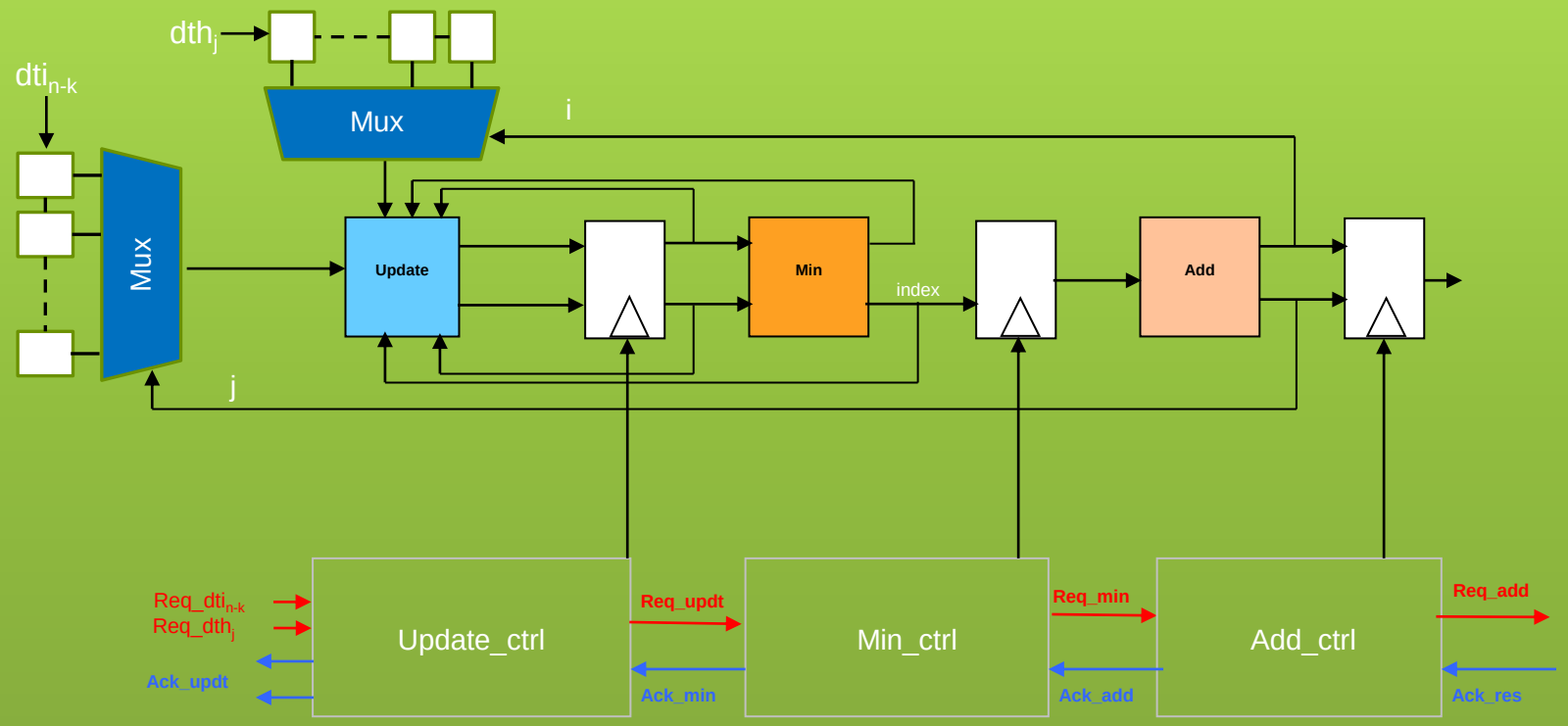
Asynchronous F.I.R filter – The conv. bloc

Architecture of the convolution product boc:



Asynchronous F.I.R filter – The test bloc

Architecture of the Test bloc:



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Conclusion & prospects

Conclusion and prospect

- Conclusion
  - Asynchronous logic is a data driven logic suitable for non-uniform sampling implementation
  - Asynchronous filtering is a more complex algorithm computed on a shorter set of samples
  - We expect to gain at least one or two order of magnitudes
  - This architecture is being implemented on an FPGA board for power measurement
- Prospects
  - Implementation with non uniformly sampled filter response
  - An automatic asynchronous filter generator tool should be developed based on non-uniform sampling

Thank you