Eiropas Reģionālās attīstības fonda projekts

2.1.1.1. aktivitāte „Atbalsts zinātnei un pētniecībai”

Projekts Nr. 2010/0283/2DP/2.1.1.1.0/10/APIA/VIAA/084

Daudzfunkcionāla signālu laika analizatora eksperimentāla izstrāde

Projekta zinātniskais vadītais – Dr. J. Artjuhs

Aktivitāte:

1.2. Jaunu attīstītu metožu, pielāgojamu specifisku pielietojumu īpatnībām, izstrāde un izpēte notikumu plūsmu efektīvai piesaistei pie reālā laika skalas

Rezultatīvais indikators

Eksperimentālais makets Nr.004/2012-ERAF

Nosaukums: GPS pieskaņotās References Frekvences Modulis

Īss apraksts: GPS pieskaņotās References Frekvences Moduļa pamatuzdevums ir nodrošināt precīzu un augsti stabilu 10MHz frekvences signālu, kontrolētu ar GPS satelītu signāliem. Modulis tiek izmantots Laika Analizatora eksperimentālā paraugā lai nodrošinātu mērījumus ar pikosekunžu precizitāti un piesaisti pie reālā laika skalas.

Modulis ir izmantojams arī citas mērīšanas un ģenerēšanas ierīces, kur vajadzēja stingra sinhronizācija un augsta precizitāte.

Tehniskie dati:

- Izejas signāls 10MHz LVCMOS (BNC konektors)
- Izejas signāls 10MHz sinusoīda 9dBm 50Ω pretestībā (SMA konektors)
- Izejas ziņojumi caur RS232 interfeisu saskaņa ar GPS uztvērēja NMEA 0183 protokolu
- Ieejas MCX GPS antenas konektors (12 kanālu GPS uztvērējs, frekvences josla L1/1575MHz, C/A kods); Antena: aktīvā ar minimālo 10dB pastiprinājumu; antenas spriegums: 2.7 – 13.2 V DC; antenas maksimāla darba strāva <=45mA;
- Ieejas 10MHz ārējais references avots (BNC konektors)
- OCXO RMS fāzes troksnis: 10Hz-2MHz 1ps Typ.
- Nominālais spriegums: +5.0V DC
- Darba temperatūras diapazons: 0-70^{o} C

(Pielikums pievienots)

Izpildītājs: Armands Mezeriņš

Izstrādāšanas un izgatavošanas laiks (no/līdz): 09.2011 – 02.2012

Izstrādes vadītājs (paraksts un atšifrējums): _____/V.Bespaļko/

Pielikums

Darba materiāli saistīti ar maketu Nr.004/2012-ERAF

EXPERIMENTAL GPS DISCIPLINED REFERENCE FREQUENCY MODULE.

The main purpose of the GPS Disciplined Reference Frequency (GPSDRF) module is to generate a 10 MHz reference frequency with a high degree of stability and precision and support high performance operational characteristic of Multi-functional Time Analyser.

GPSDRF module is developed on basis of FTS375-010.0M Disciplined Reference and Synchronous Clock Generator hybrid circuit. The FTS375 module is GPS disciplined phase-lock loop circuit providing the 1 PPS CMOS output from GPS timing receiver and generating 10MHz CMOS and 10MHz sinusoidal signals from intrinsically low jitter Voltage Controlled Crystal Oscillator. The FTS375 module can synchronize the outputs to following references:

- 10MHz derived from the on-board ConWin GPS timing receiver,
- external 10MHz reference, or
- external 1PPS reference.

Outdoor mounted GPS antenna is necessary to provide consistent performance.

The FTS375 module has indications of Lock, Holdover and Antenna Fault states. Two inputs SYNC1 and SYNC2 for a mode control are used for manual switching between references or force holdover (provided by OCXO oscillator) in dependence on monitored Lock, Holdover or Antenna Fault alarm states.

GPSDRF module is implemented as a print circuit board with 10MHz LVCMOS reference input, GPS antenna input and the following outputs:

- 10MHz sinusoidal for the time base of the Multi-functional Time Analyser,
- 10MHz LVCMOS for laboratory use, and
- serial interface RS232 input/output lines providing an access to the NMEA messages from GPS receiver (can be used to access GPS timestamp information, verify that receiver has recovered from an alarm condition, connect with another modules etc.).

A behavioural algorithm of the GPSDRF module includes following steps: MCU PIC18 microcontroller provides initial settings for FTS375 circuit – sets GPS receiver as default reference source, then successful synchronization to one of contrary states: Lock or Holdover, which are indicated by relevant LEDs; in presence of the external 10MHz LVCMOS signal at external reference input the microcontroller sets this reference as the main reference source and correspondingly indicate possible Lock or Holdover states with LEDs.

The GPSDRF module prototype for Multi-functional Time Analyser is designed accordingly the architecture illustrated in figure 1. The GPSDRF module consists of :

1) FTS375-010.0M hybrid circuit;
2) PIC18F24K20 microcontroller unit provide initial setup and monitoring functions;
3) MAX202 transceiver circuit for RS232 to TTL level conversion.

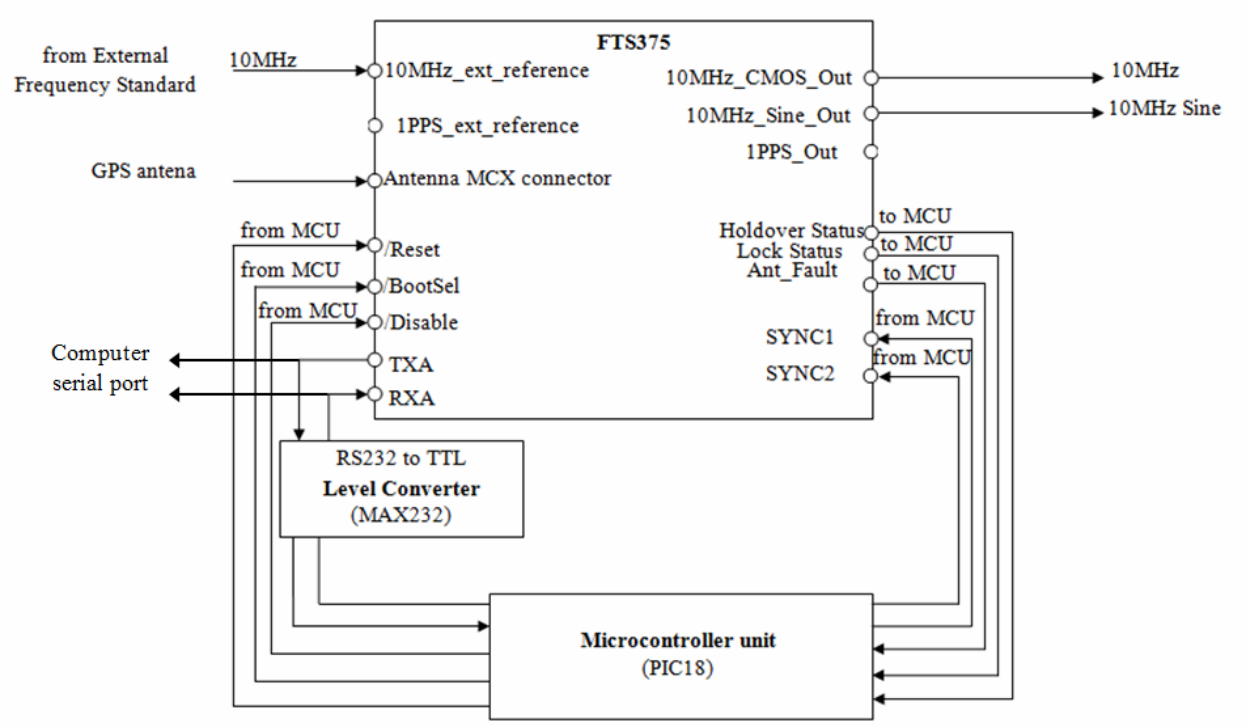

Figure 1. System architecture

An indication of module operating modes is provided by four red SMD LEDs placed on the prototype circuit board:

- LED1 blinking – module is active;
- LED2 blinking – the external 10MHz is set as a reference source, LED2 is continuously ON – module is synchronized by the external 10MHz and transitioned into the Lock state;
- LED3 is continuously ON – the module is transitioned into the Holdover state;
- LED4 blinking – GPS receiver is set as a reference source, LED4 is continuously ON – the module is synchronized by the GPS signal, derived from the GPS satellites, and transitioned into the Lock state.

Figure 2. GPS Disciplined Reference Frequency module experimental model

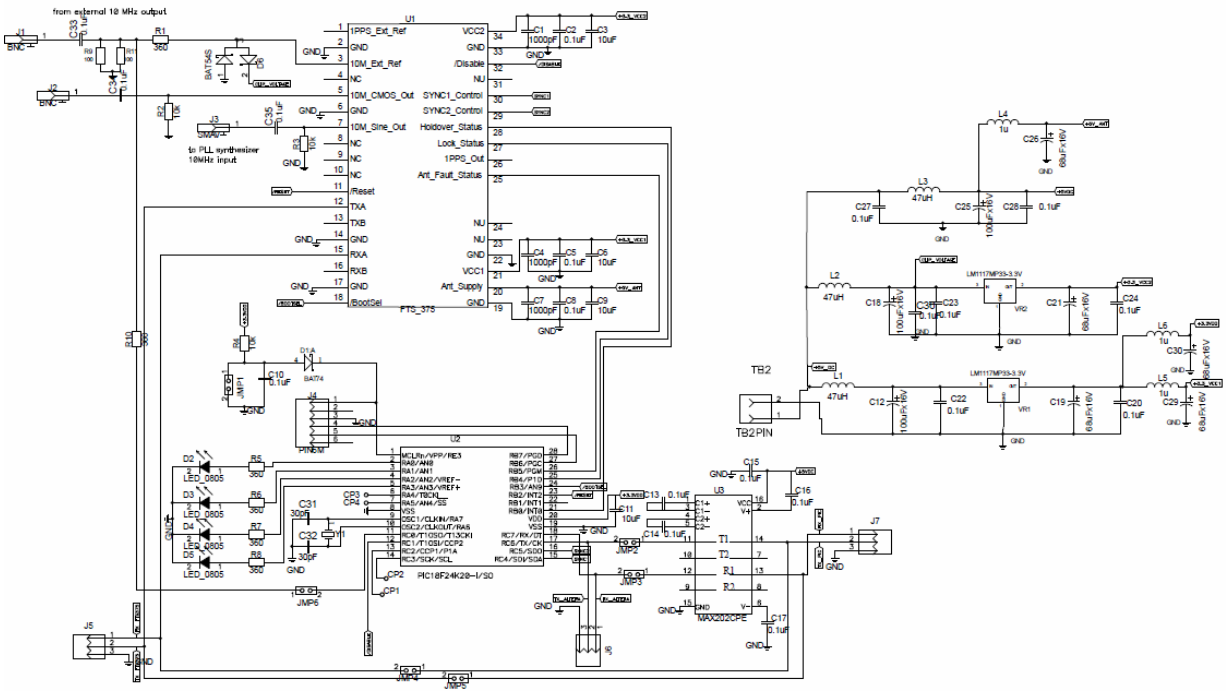

Figure 3. GPSDRF module circuit diagram

MEASUREMENTS AND EXPERIMENTAL DATA

The results of experimental estimation of Reference Frequency stability by means of Event Timer A033-ET measurements are illustrated in figures below.

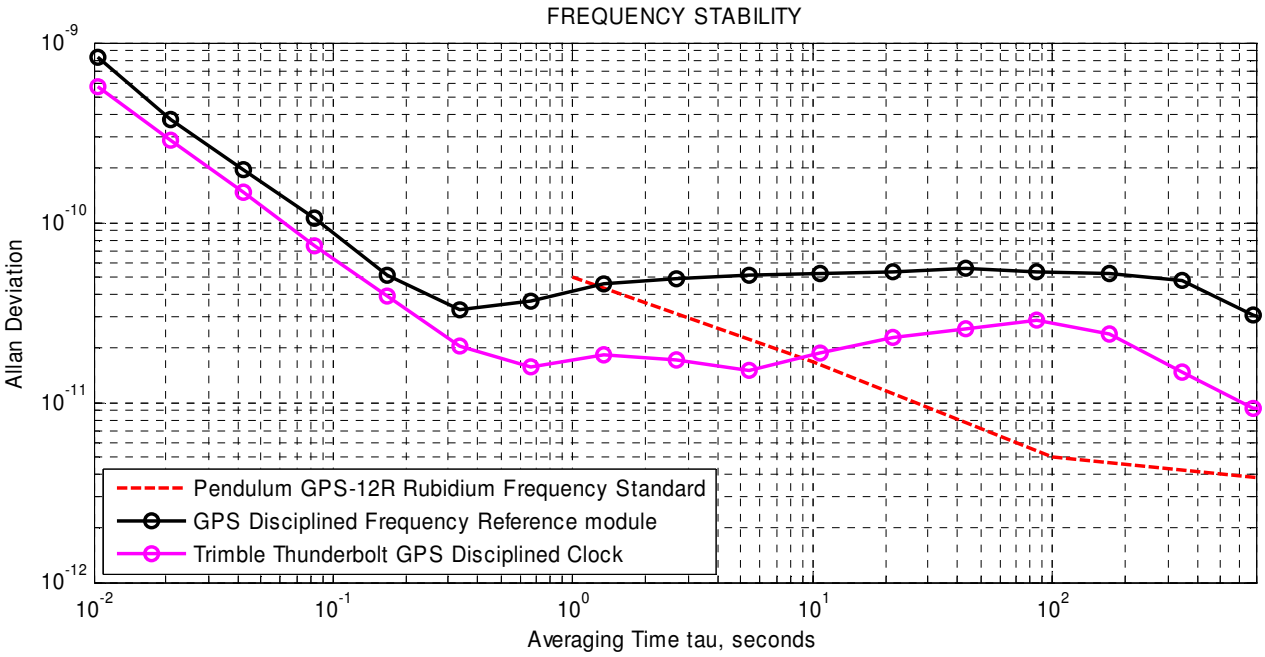

Figure 4. Frequency stability of GPS Disciplined Reference Frequency module compared to nominal stability of GPS-12R (from specifications) and measured Trimble Thunderbolt GPS Disciplined Clock present in laboratory

Figure 4 shows the time stability (Allan Deviation - ADEV) of estimated GPS Disciplined Reference Frequency module with respect to Rubidium standard available in laboratory, and for comparison measured stability of Trimble Thunderbolt GPS Disciplined Clock, and stability data from Rubidium standard specification.

Figure 5 shows the ADEV of a GPS Disciplined Reference module when free running (not locked to GPS signal) and the actual stability when disciplined to the GPS signal.

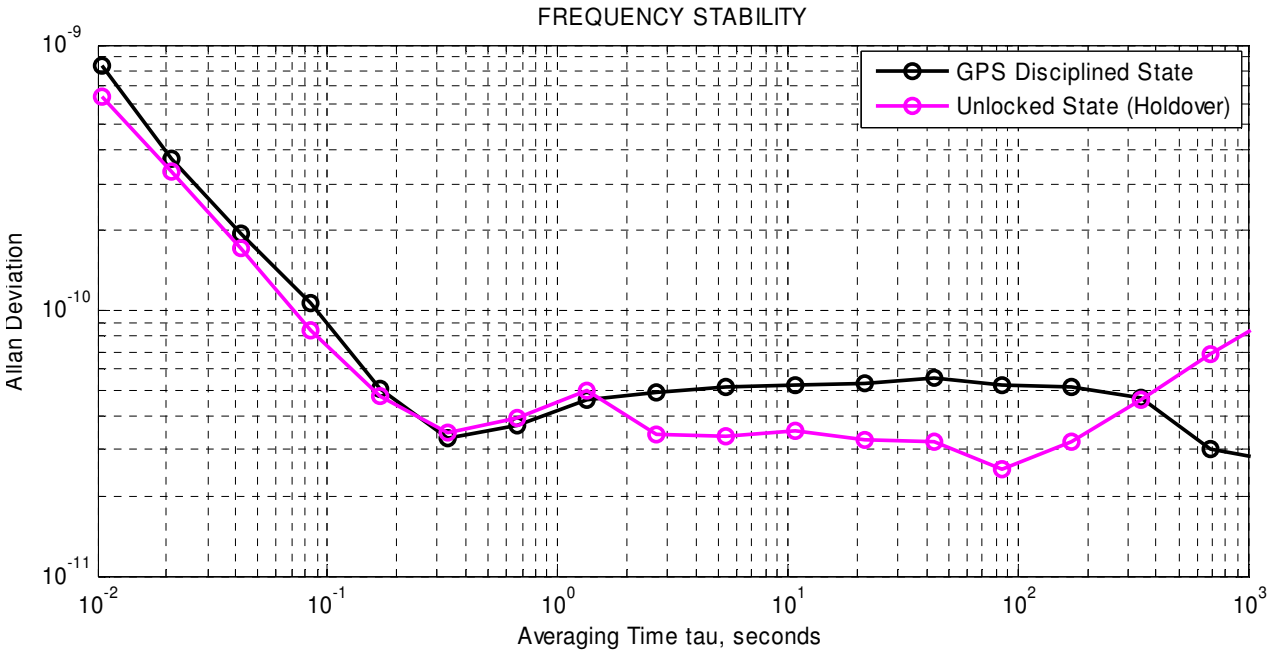

Figure 5. Frequency stability of GPS Disciplined Reference Frequency module in disciplined state compared to holdover (undisciplined, essentially the performance of the internal OCXO)

ADEV illustrates oscillator performance versus time – all graphs use the same scales: on X-axis are decades of averaging time – from 10 milliseconds up to 1000 seconds; y-axis are decades of relative stability from 10^{-9} to 10^{-11}. Quartz oscillators have excellent phase noise (jitter) in the short term, but when measured over interval of minutes there is observed significant random walk of frequency. The main idea of GPS disciplined oscillator is to allow the quartz free run before the phase of random walk, what could be controlled with the time constant of servo loop. We can see that disciplined oscillator diverges from undisciplined oscillator at a time interval near 350 seconds.

The negative descending slope of white noise region is in the first fractional parts of seconds, then becomes visible significant variation of wander or flicker floor region (slope 0). Next at 100 seconds in undisciplined graph dominates random walk noise. We can observe that GPS corrections remove from the oscillator performance variations introduced by aging and frequency random walk. In synchronization mode Allan deviation line after 300 seconds monotonically decreases to its nominal value, stability rapidly improves within parts of 10^{-14} and is kept in continuous agreement with GPS. The nature of this variation is white noise raised by selective availability and it eliminates a random walk or flicker noise seen from undisciplined ADEV graph.