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EIROPAS SAVIENĪBA
Eiropas Reģionālās attīstības fonds

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Projekts "Laika sinhronizācija ar augstu precizitāti sadalītai zinātnisku mērījumu sistēmai"

Vienošanās ar Centrālo finanšu un līgumu aģentūru Nr. 1.1.1.1/16/A/174

Takts izplatīšanas sistēma telpā sadalītiem reģistratoriem
Tehniskā specifikācija

Aktivitāte Nr.1.4.

ELEKTRONIKAS UN DATORZINĀTŅU INSTITŪTS
INSTITUTE OF ELECTRONICS AND COMPUTER SCIENCE

Elektronikas un datorzinātņu institūts

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Kopsavilkums

Šī specifikācija ir projekta aktivitātes 1.4 “Takts izplatīšanas sistēma telpā sadalītiem reģistratoriem” rezultāts. Aktivitātes ietvaros ir izpētītas prasības pret pulksteņu sinhronizāciju telpā sadalītu sensoru tīklam, izstrādāti sistēmas darbības principi un to realizācija aparatūras prototipā, noteikti tās darbības raksturlielumi un parametri. Aktivitāte 1.4 ir cieši saistīta ar aktivitāti 2.4 “Takts signāla izplatīšanas sistēma neitrīno detektoram,” kuras ietvaros izstrādāts sistēmas eksperimentāls makets. Specifikācija apraksta arī sistēmas realizāciju maketā.

Takts izplatīšanas sistēma telpā sadalītiem reģistratoriem piedāvāta izmantošanai starptautiska projekta “Jiangmenas pazemes neitrīno observatorija” (JUNO) ietvaros
(skat. https://en.wikipedia.org/wiki/Jiangmen_Underground_Neutrino_Observatory).

5 lpp., 3 zīm. (angļu valodā)

Local Clock Distribution System (LCDS)

1. System description

LCDS is intended for industrial or scientific experimentation systems that are used to collect timing information from multiple sensors, which are remote and specially distributed. Such systems very often have time measurement devices (event timers or, in other words, time-tagging devices), which sit close to each sensor. Each time-tagging device has its own local time-scale. The signals from the sensors that are regarded as informative events are time-tagged and then the obtained time-tags are transmitted to some central data acquisition unit. The time-tags that are related to different sensors later have to be placed on some single system time scale so as to be correctly processed for the experimental or industrial needs. Sometimes it is needed to have the time-tags associated with the UTC (Coordinated Universal Time).

The proposed LCDS has to cover the above mentioned needs and provides the following functionality:

1. Provision of the stable synchronous clock for all local time-tagging devices.
2. Synchronization (syntonization) of all local timescales of the local time-tagging devices.
3. The calibration of the timing offsets between all measurements channels (global calibration).

And additionally, if the True Event Timing is required:

4. Provision of a System Time Scale, which is synchronized with the UTC.
5. Absolute timing calibration. It means that all timestamps from different channels have to be UTC associated.

The LCDS consists of the following main blocks: Time and Frequency Standard (TFS, often it is called Time and Frequency Reference), Central Clock Distribution Unit (CCDU), Fan-out drivers, and Local Time-tagging Devices (strictly speaking they are not part of the system, shown only for the clarity of the description). The block diagram of the LCDS is shown in Fig. 1.

The operation of the system is based on the use of a TFS. The TFS produces a stable clock signal (10 MHz as a rule) alongside with the Time Code signal (IRIG-B standard is suggested to be used as one

of most popular). Such device normally can be disciplined from the GPS network and is usually based on a Rubidium standard or a TCXO (temperature compensated crystal oscillator). The CCDU produces

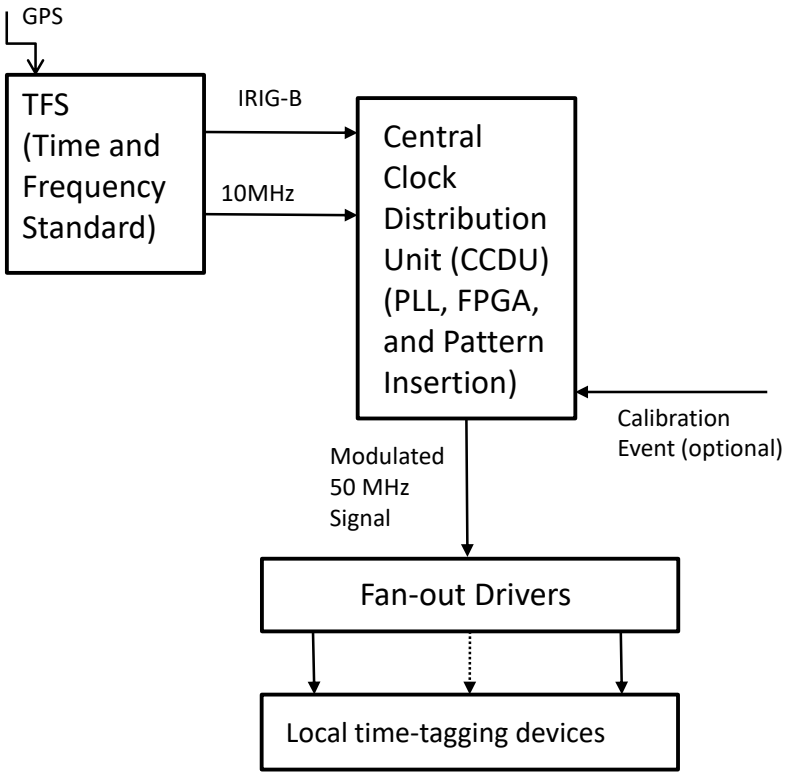

Fig. 1. Block diagram of the Local Clock Distribution System.

a very stable and low jitter 50 MHz clock signal that is farther distributed by Fan-out Drivers. Upon the reception of the time code from the TFS, the CCDU inserts a specific code pattern in the 50 MHz signal. The local time-tagging devices use the 50 MHz signal to build their internal time-scales. The synchronization (strictly speaking – syntonization) is done with the use of the inserted time codes that are repeated (typically – once in a second). The time code contains the current UTC time, a specific edge of the pattern indicates the 1PPS signal. The local time-taggers have to be equipped with Clock and Data Recovery (CDR) blocks that are PLL (phase-locked loop) based and are able to extract time codes from the incoming 50 MHz signal.

It is evident that, because of different delays between the CCDU and the local time-tagging devices, the local time scales always have different time offsets between each other. Therefore to perform time-tagging of the events that are related to different local time-scales, the global system calibration has to be performed. Normal way to do that is to generate a special physical pulse signal that has the impact on all sensors of the time measurement system. In optical systems, for example, such signal could be a flash of a laser or LED (Light Emitting Diode) that is received by all sensors. The spatial position of the calibration signal source has to be determined (or accurately measured). The calibration procedure is illustrated in the Fig. 2.

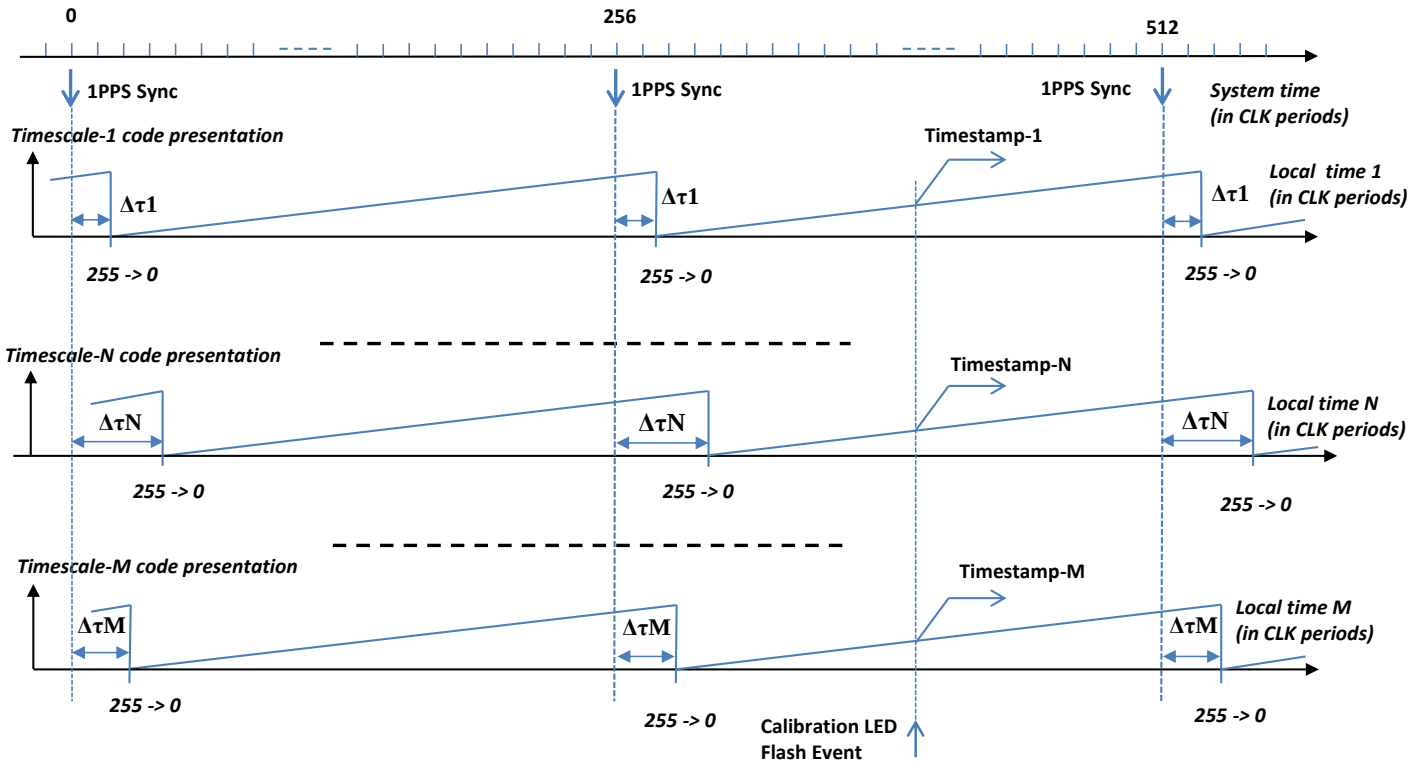

Fig. 2. Global synchronization principle.

The calibration events (caused by flashing the central LED) are time stamped by all local time-tagging devices with respect to their local timescales. These timestamps (Timestamp-1,…, Timestamp-n,…, Timestamp-M) are offset with respect to one another. And not only the offsets between the local timescales get included in those offsets of the timestamps, but also the different delays along the optical-electronic paths of LED Flash Event before the timestamps are taken by different local time-

taggers (optical length delays, delays of the front-end sensors, delays of input amplifiers, etc.). So, all delays are included and can be taken into account by means of the Global Calibration. This way all time-tags from local time-taggers become related to some single system local time-scale, which, it its turn, can be associated with the UTC.

2. Central Clock Distribution Unit description

A compact implementation of the CCDU is based on the use of a generic FPGA. The CCDU consists of a Comparator, a FPGA, a PLL Low Pass Filter (PLL LPF), a 100 MHz VCXO, and a Code Manipulation Circuitry (CMC). A block diagram of the CCDU is shown in Fig. 3.

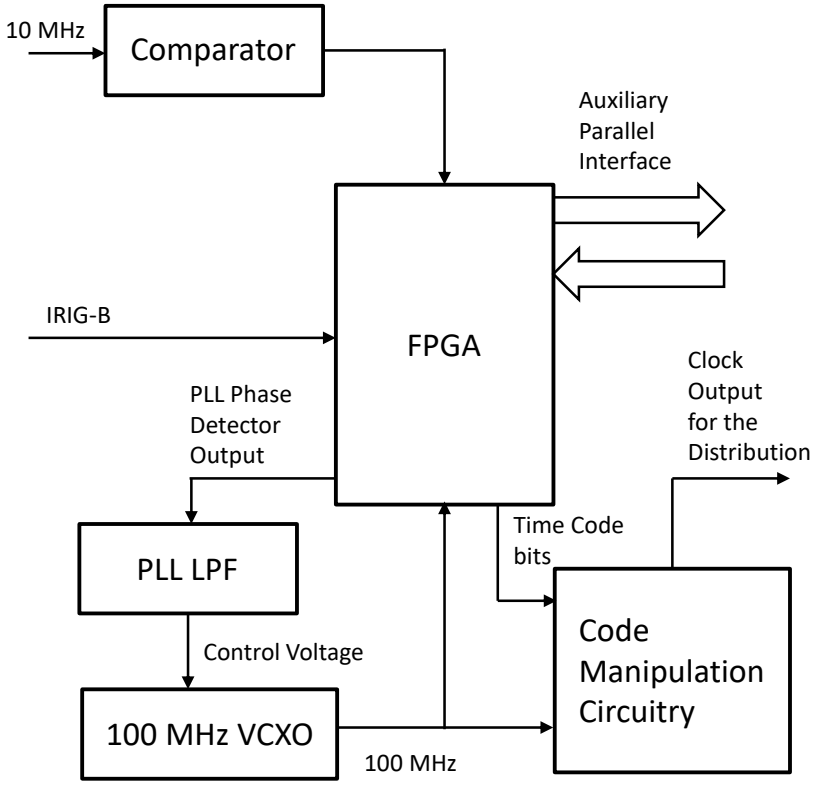

Fig. 3. Block diagram of the Central Clock Distribution Unit.

The Comparator performs conditioning of the 10 MHz input signal (it could be a pulse or sinusoidal signal with different amplitude). The LVTTL signal from the output of the Comparator comes to the

FPGA. The generation of the 100 MHz on-board internal clock (up-conversion of the 10 MHz to 100 MHz) is done by the PLL circuitry, which is implemented inside the FPGA. Only PLL LPF is done outside the FPGA. The PLL LPF produces the control voltage for the 100 MHz VCXO to obtain the locked loop. As a result the obtained 100 MHz clock signal is synchronized to both the input 10 MHz signal and the IRIG-B signal. The 100 MHz clock is fed both to the FPGA and the Clock Manipulation Circuitry. The CMC is implemented on the basis of a D-type flip-flop circuitry. When the IRIG-B 1PPS signal comes, it is processed by the FPGA that inserts a specific pattern into the output clock by the provision of information bits (which come to the D-input of the main flip-flop of the CMC).

3. CCDU realization and obtained specifications

The CCDU is implemented as a single board 90mm x 107mm (see a photo in Fig. 4). The Altera CycloneII FPGA (EP2C5T144C7) is used. The board can be used in different distributed time-tagging

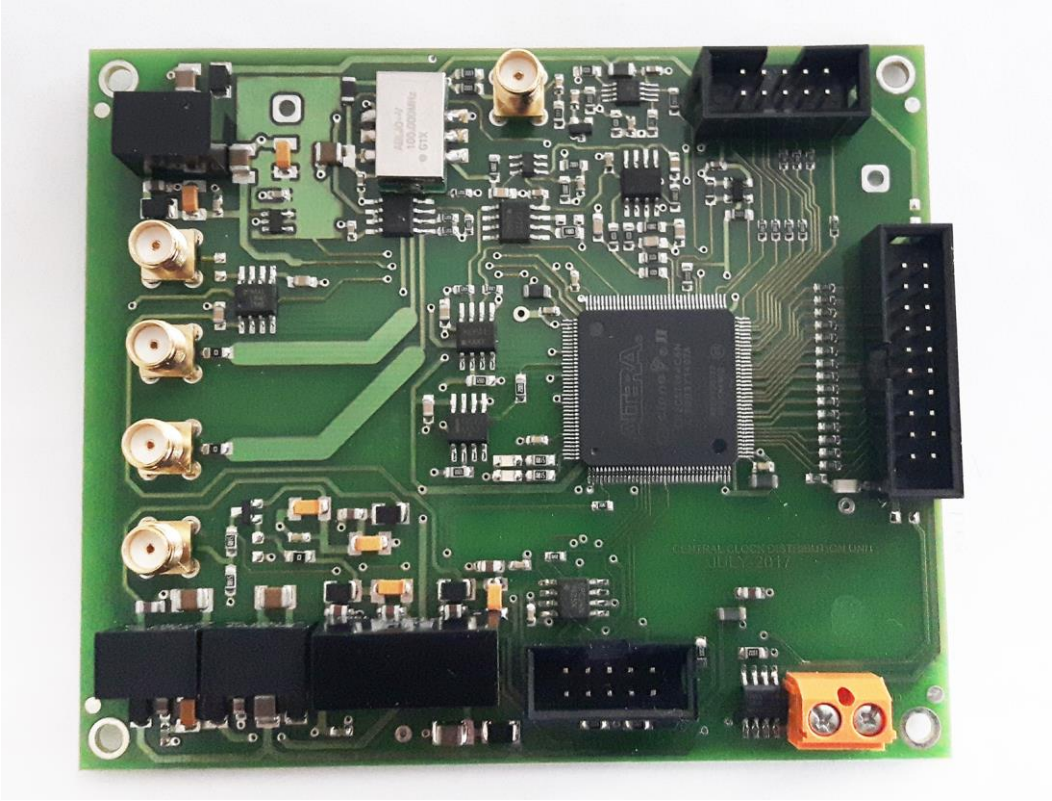

Fig. 4. Photo of the CCDU.

systems and adjusted for the use of different distributed clock frequencies. The distributed clock frequency depends on the selected VCXO frequency and clock division coefficients that could be modified in the VHDL code for the FPGA.

The schematic of the CCDU as of Fig.3 is given in the files Proto24_1_FPGA.pdf, Proto24_2_PLL.pdf, and Proto24_3_Power.pdf. Block Comparator is realized on the IC U16 (ADCMP602), the input stage is equipped with the voltage limiting diodes D11. The FPGA block is realized on the IC U14. Block PLL LPF is implemented with the use of the IC U17 (OPA347). The Code Manipulation Circuitry is done by the ICs U1, U21, U2. The VCXO is the IC U19. The CCDU is powered by a single supply +5V, the required (by the ICs) power supply voltages (+3.3V, +1.2V, -5V) are obtained from the secondary voltage regulators (U22, U23, U25, U26, and U27).

The main specifications of the designed board are:

- Reference signal (10 MHz) input – AC, 50 Ohm input impedance, 100mV-10V peak-to-peak
- IRIG-B input – LVTTL, 50 Ohm input impedance
- Auxiliary parallel interface - LVTTL
- Auxiliary system clock output – differential LVPECL
- Output distributed clock signal – LVTTL, 50 Ohm diving capability
- Output clock signal jitter – less than 3 ps
- Distributed clock frequency range – 10-200 MHz
- Time code insertion format – IRIG-B
- Size - 90mm x 107mm
- Power supply +5V, 450 mA

The board was tested and showed reliable operation. The distributed clock jitter was measured indirectly by the use of two test 100 MHz PECL outputs (differential signals). These signals were connected to the main board of the Eventech A033-ET (high accuracy event timer with the time-tagging RMS resolution less than 2 ps) and used as the system clock of that event timer. Then time measurements (by the A033-ET) of a low jitter pulse signal were carried out. The results showed a small time-tagging RMS resolution degradation (3 ps instead of the specified 2 ps), which means that

the jitter of the CCDU system clock is less than 3 ps (based on the assumption that the A033-ET is "ideal" and introduces no measurement error, which is not true). So, in the reality, the jitter of the CCDU clock is noticeable lower. But this guaranteed figure of jitter is much better then typically required. As a rule the distributed clock signal degrades in the transmission lines and driving/receiving circuitry and then the jitter is improved in the CDR (clock data recovery) units of local time-taggers (the degree of such improvement depends on the application).

Abbreviations and terms

AC – Alternate Current
CCDU - Central Clock Distribution Unit
CDR - Clock Data Recovery
CMC - Code Manipulation Circuitry
FPGA - Field-Programmable Gate Array
GPS - Global Positioning System
IRIG-B - Inter Range Instrumentation Group time code format B
IC – Integrated Circuit
LCDS - Local Clock Distribution System
LED - Light Emitting Diode
LVPECL - Low Voltage PECL
LVTTL – Low Voltage Transistor–Transistor Logic
PECL - Positive Emitter-Coupled Logic
PLL LPF – Phase Locked Loop Low Pass Filter
PPS – Pulse Per Second
RMS – Root Mean Square
Syntonization - setting clock signals to the same frequency (rate), regardless of the phase
TCXO - Temperature Compensated Crystal Oscillator
TFS - Time and Frequency Standard
UTC - Universal Time Coordinated
VCXO – Voltage Controlled Crystal Oscillator
VHDL - Very High Speed Integrated Circuit Hardware Description Language