INSTITUTE OF ELECTRONICS AND COMPUTER SCIENCE

RIGA EVENT TIMER IN COMPACT IMPLEMENTATIONS

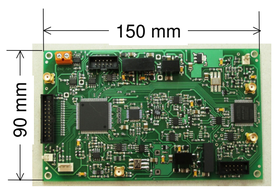
In complex systems, a timing block is often required as a compact module that can be built in a common housing together with other functional modules. To meet these requirements we have developed the set of the event timing modules with different performance and precision. The modules also differ with schematic complexity, sizes and power consumption.

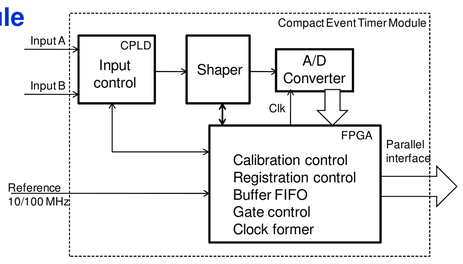
Compact Event Timer Module (CETM) provides the same functionality as A033-ET while the size of board is only 90x150 mm and power consumption 4 W. The modified interpolator has dead-time 25 ns providing for measurement rate up to 40 MSPS. This modification allows the wider range of external conditions however degrades the resolution up to 5 ps RMS.

Doubled Event Timer Module presents two CETM's integrated into one module.
Two separate interpolators for two inputs Start and Stop provide independent registration of events arriving in these inputs allow measuring of zero or negative time intervals between these events. The size of board is 120x160 mm and power consumption is about 5 W.

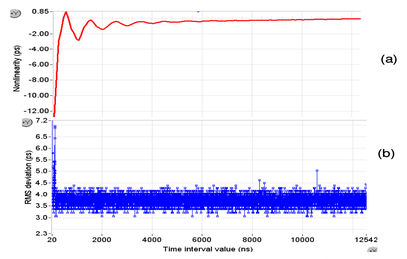
Fast Event Timer Module is the timing module providing one channel measurement with very high frequency up to 90 MSP and resolution about 5 ps. In case of low event rates this resolution can be enhanced up to 2.5 ps using the replication possibility. A preliminary size of board is 160x220 mm however it can be essentially minimized. The power consumption is 8 W.

Compact Event Timer Module

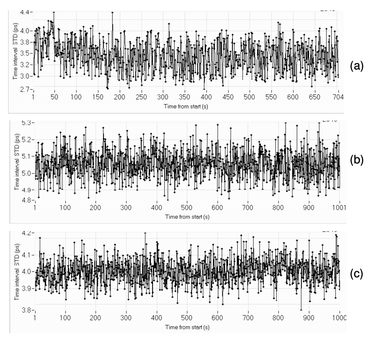




Functional diagram of Compact Event Timer



Interval non-linearity error (a) and RMS resolution (b) dependence on time interval value

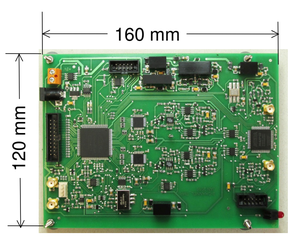


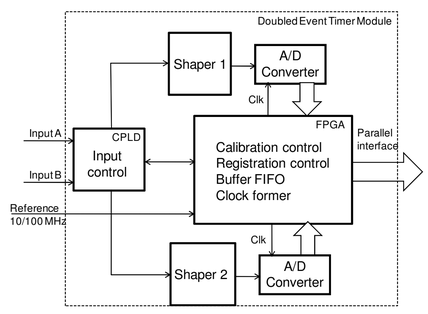
CETMS interpolator has two different time-to-digital conversion schematics for odd and for even events. This allows maximal reducing of the dead-time but increases the random error for interval between odd and even events.
Test results on the left show the RMS resolution values and stabilities for intervals between:
(a) only odd events;
(b) only even events;
(c) odd and even events.

Pro: - compactness: 90x150 mm
- small power consumption: 4 W
- the module is ready for operation immediately after assembly
- fast and stable calibration
- high resolution – 4-5 ps RMS
- short dead-time – 25 ns

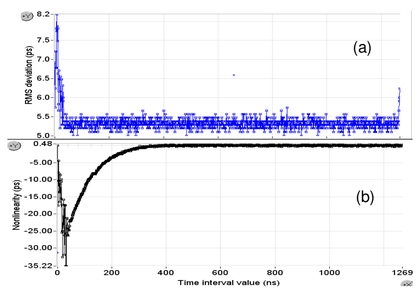
Contra: - essential interval non-linearity for short intervals
- two interpolators require two conversion tables and double random error variance

Doubled Event Timer Module





Functional diagram of Doubled Event Timer



Interval non-linearity error (a) and RMS resolution (b) dependence on time interval value

DETM incorporates two CETMs with one shared CPLD for input control and one FPGA for parallel functionality. DETM development was aimed to time almost simultaneous events which are typical for Positron Emission Thomography devices in medicine and particle registration in nuclear physics.

In the DETM each interpolator has just one time-to-digital conversion schematic and provides the RMS resolution 4 ps but for Start-Stop intervals the error variance is summed from both interpolators and resulting RMS resolution is 5.5 ps.

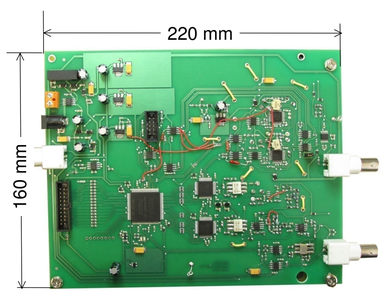
For short intervals less than 30 ns this resolution degrades up to 8 ps because of cross-correlation of close events.

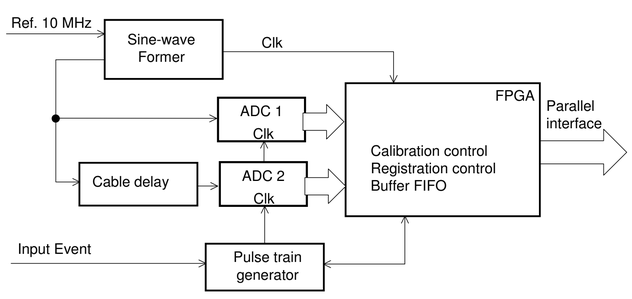
The same effect impacts to the non-linearity error but it can be identified simultaneously with the channel-to-channel offset and corrected in the interval calculation.

Pro: - compactness: 120x160 mm
- small power consumption: 5 W
- the module is ready for operation immediately after assembly
- fast and stable calibration
- high resolution – 5-6 ps RMS
- no dead-time for different inputs

Contr: - RMS resolution degradation up to 8 ps for intervals less than 30 ns.
- essential interval non-linearity for short intervals
- two interpolators require two conversion tables and double random error variance

Fast Event Timer Module



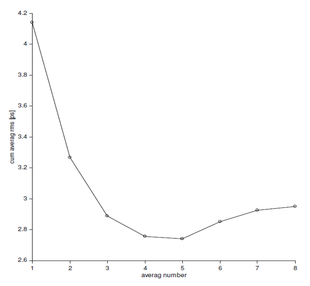


Functional diagram of Fast Event Timer

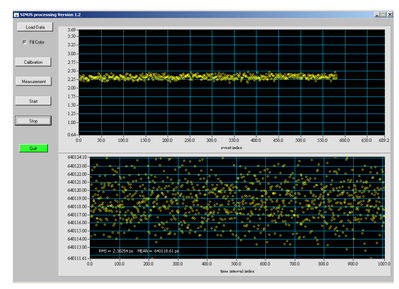
FETM is built on the basis of timing technology that differs from A033-ET technology. It uses a digital sampling of the stable sine-wave functions in time instants directly related to arriving of input events. This allow increasing measurement rate up to hundreds millions time-tags per second.

The developed pilot version can register up to 90,000,000 time-tags/sec and has an additional feature allowing to improve the RMS resolution from 5 ps for event rate 90 MHz to 2.5 ps for event rate less than 20 MHz.

FETM development was aimed to applications where increasing of timed events frequency allows increasing received or transferred data volume. The Data transfer via Laser link, LIDAR system, 3D-Scan system are such system which performance is defined by data acquisition rate and timing precision.



RMS resolution dependence on the number of refining pulses that are generated until an arrival of next event. It is seen that in this module the refinement is effective until the forth refining pulse.



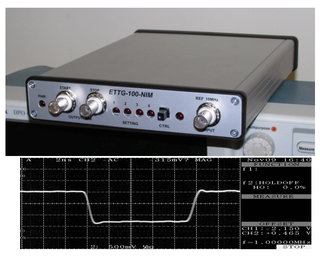
RMS resolution stability (upper) and measured time interval values (bottom). The time 640 ns between events allows to refine the time-tags and to get resolution 2.3 ps (including test generator instability).

Event Timer Test Generator ETTG-100 is designed for estimation of precision parameters of Event Timers and similar timing devices (Time Interval Counter, Time Analyzer, Time-to-Digital Converter) having a picosecond resolution of time measurements. In accordance with existing standards for inputs of timing devices, the Generator ETTG-100 has two modifications:

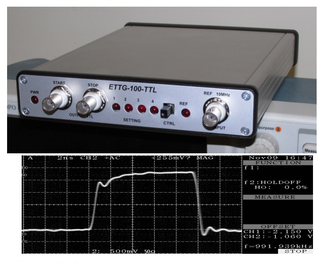
- ETTG-100-NIM generating negative pulses in NIM standard, and
- ETTG-100-TTL generating positive pulses in LVTTL standard.

ETTG generates periodic sequences, characterized by high short-term stability of the repetition period. The standard deviation of this period is about 1 ps and that allows testing timing device and systems.

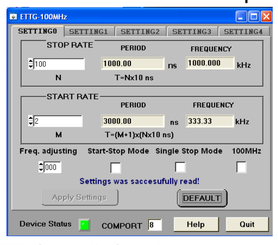
ETTG may operate in stand-alone and software controlled modes. In stand-alone mode ETTG has five settings sequentially selectable by the CTRL button. The delivered software allows via USB to change any of these settings.



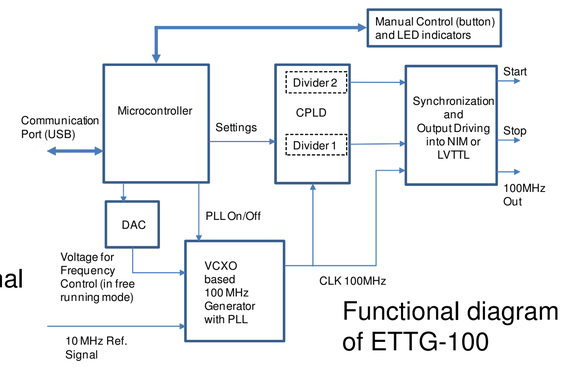
ETTG-100-NIM and its output signal



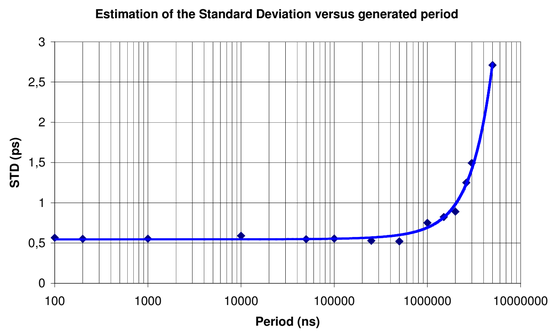
ETTG-100-TTL and its output signal



ETTG-100 Control program

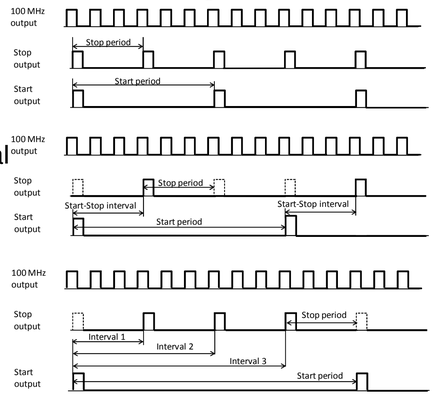


Functional diagram of ETTG-100



Experimental estimation of the ETTG period stability in the range of periods from 100 ns up to 5 ms. Experimental points present STD averaging on ~500 STD values, when each of them is estimated on the array of 1000 measured periods.

Three generation modes and their time diagrams



Period generation:
Stop period = N x "100 MHz" period
Start period = M x Stop period
"100 MHz" = 10 ns ± 0.4ps adjusting

Time interval generation:
Stop period = N x "100 MHz" period
Start period = M x Stop period
"100 MHz" = 10 ns ± 0.4ps adjusting

Multi-stop time interval generation:
Stop period = N x "100 MHz" period
Interval 1 = Stop period
Interval 2 = 2 Stop periods
Interval 3 = 3 Stop periods
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This poster reflects the research results that were obtained in the framework of the R&D project No. 2013/0036/2DP/2.1.1.1.0/13/APIA/VIAA/032 "**Universal time event recorder for SLR, LiDAR and 3-D scan applications**" partially financed by ES. Eventech Ltd., being one of the developers in this project, in 2016 at an auction acquired the exclusive right to further production and distribution of devices developed under this project.

E. Boole, V.Bespalko, A.Rybakov, V.Vedin, Institute of Electronics and Computer Science; buls@edi.lv; ***R. Spunde*** (Eventech Ltd., Riga, Latvia; r.spunde@eventechsite.com)